Tips on High Speed Digital Design

by

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High Speed Scenario

- Effect of passive circuit elements - wires, IC packages, PCBs.
  - Signal propagation (Reflection & ringing)
  - Interaction between signals (crosstalk)
  - Interaction with natural world (EMI)

Knee Frequency

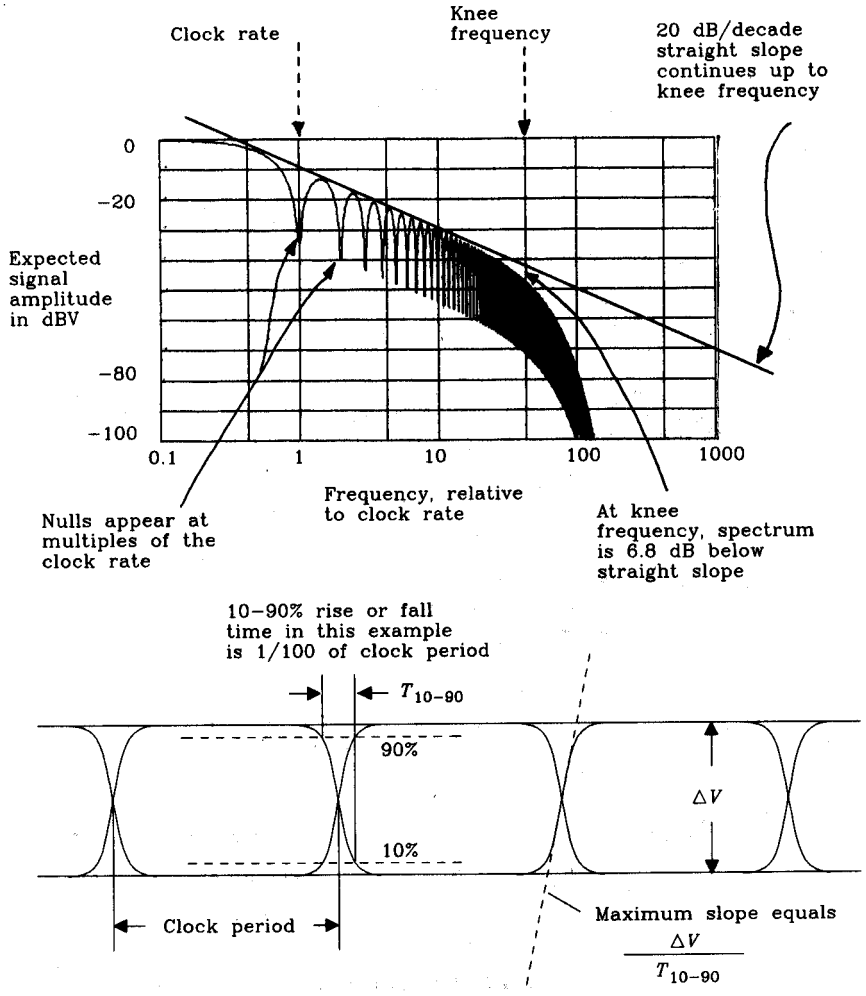


Figure 1.1 Expected spectral power density of a random digital waveform.

$$F_{knee} = \frac{1}{2T_r}$$

–Not a substitute for Fourier analysis

–Precise risetime measurement

–EM emissions depend upon spectral behavior well above F_{knee}

Time and Distance

- Propagation delay is proportional to the square root of the dielectric constant.
- The propagation delay of signals traveling in air is 85 ps/in.
- Outer-layer PCB traces are always faster than inner traces.

Lumped Vs Distributed systems

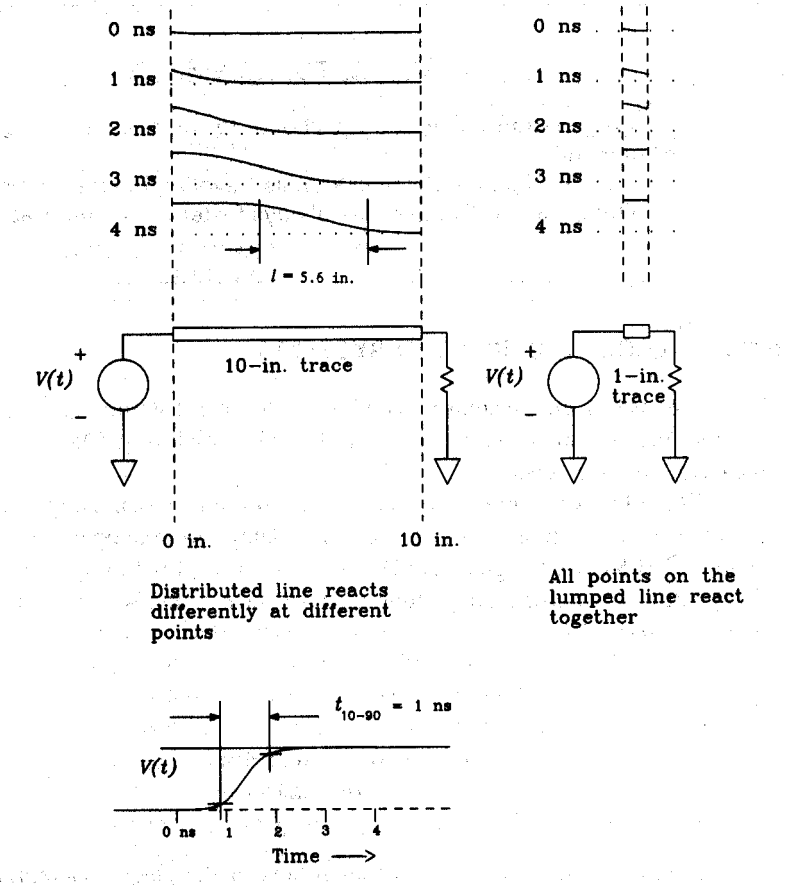


Figure 1.3 Snapshots in time of the electric potential on distributed and lumped transmission lines.

$$l=\frac{T_r}{D}$$

For PCB traces, point to point wiring and bus structures,

- length < l/6 - Lumped
- length > l/6 - Distributed

High speed properties of Logic Gates

- Power
- Speed
- Packaging

1. Standard packaging - money, flexibility, limits number of pins and gates per package, partitioning, power and speed constraints

2. Max power dissipation per package - package, cooling properties

3. Speed Vs Power

Power

- Input Power
- Internal dissipation
- Drive Circuit dissipation
- Output power

Quiescent and Active components

Power in Logic Gates - Categories

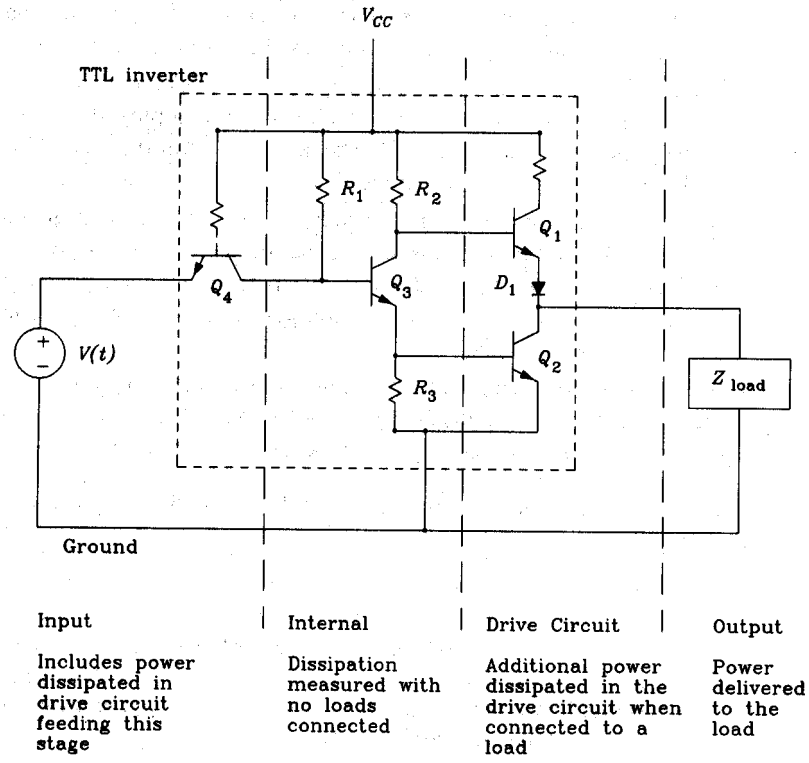
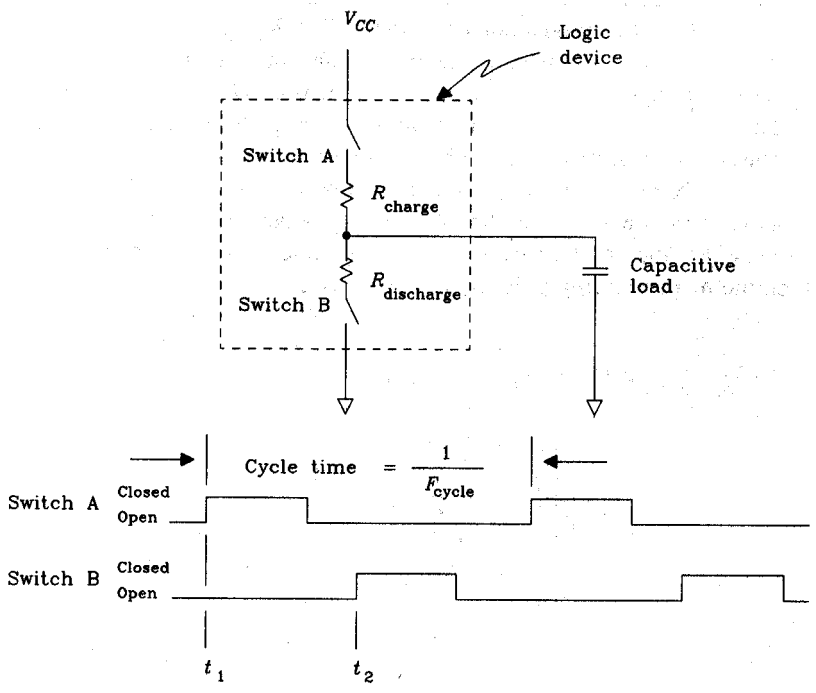


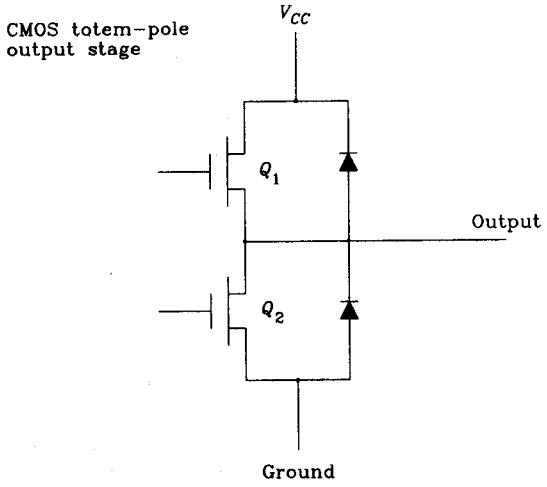
Figure 2.1 Categories of power dissipation in and around a logic device.

Active power dissipation when driving a Capacitive load



$$P_{active} = FCV_{cc}^{2}$$

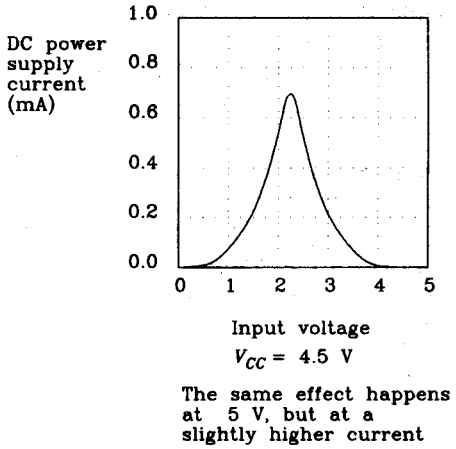
Active Power - Overlapping Bias currents



Less in Schottky

CMOS, TTL, ECL

DC consumption of Signetics 74HC00 family



At intermediate input levels both output transistors remain on simultaneously, drawing excess current from the power supply

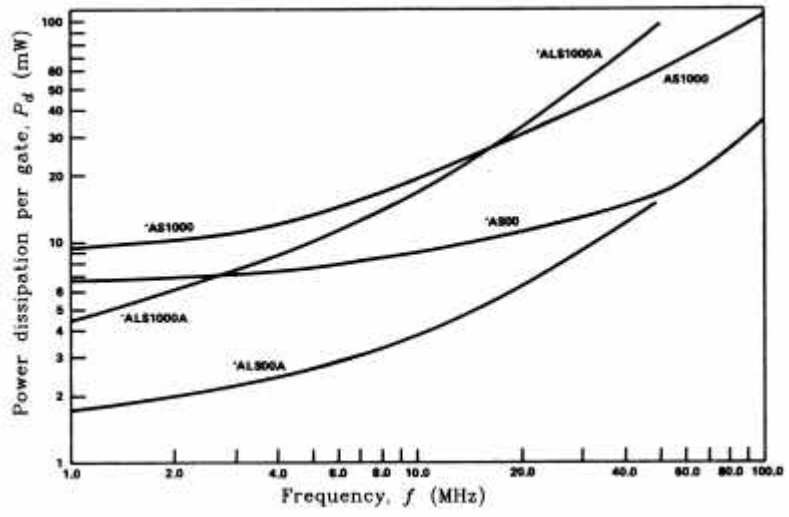
The same effect happens at 5 V, but at a slightly higher current

Input Characteristics of Logic Families

TABLE 2.1 INPUT CHARACTERISTICS

	74HCT00	74AS00	10H101	10G001
I_{in}HI (mA)	0	+0.020	+0.425	+0.400
I_{in}LO (mA)	0	–0.500	+0.0005	–0.100
$P_{quiescent}$(mW)	0	1.3	1.1	1.3
C_{in} (pF)	3.5	3	3	1.5
ΔV_{in}(V)	5.0	3.7	1.0	1.5
P_{active}(mW)				
F = 1 MHz	0.09	0.04	0.003	0.003
F = 10 MHz	0.9	0.4	0.03	0.03
F = 100 MHz			0.3	0.3
F = 1000 MHz				3.0

Internal Power dissipation

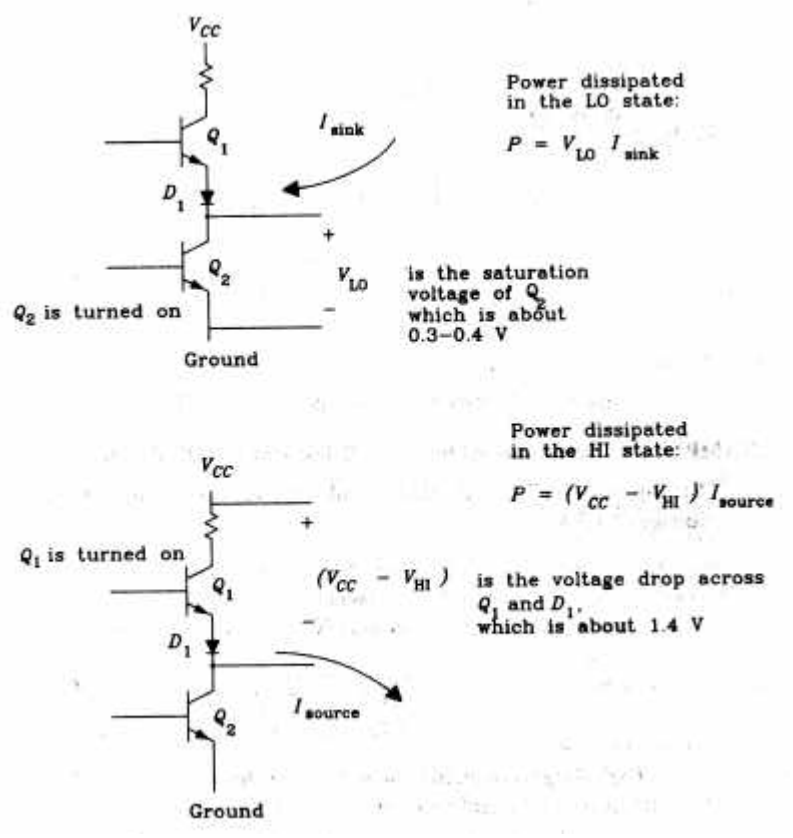


$$K_{active} = \frac{P_{total} - P_{quiescent}}{F}$$

Drive Circuit Dissipation

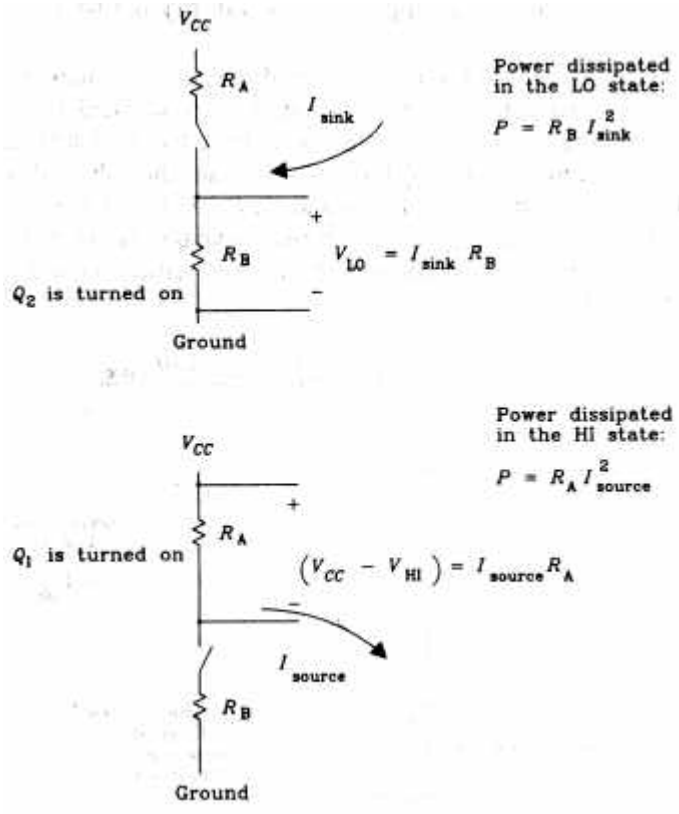
- Totem pole
- Emitter follower
- Open Collector
- Current Source

Quiescent Power - Totem-pole output circuit

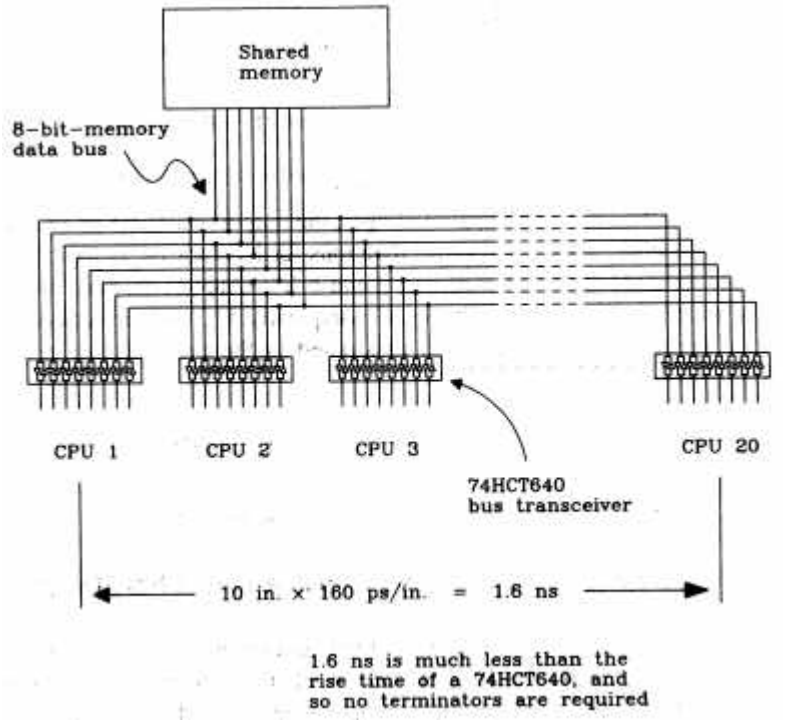


$$P_{quies} = \frac{0.4 I_{Sink} + 1.0 I_{Source}}{2}$$

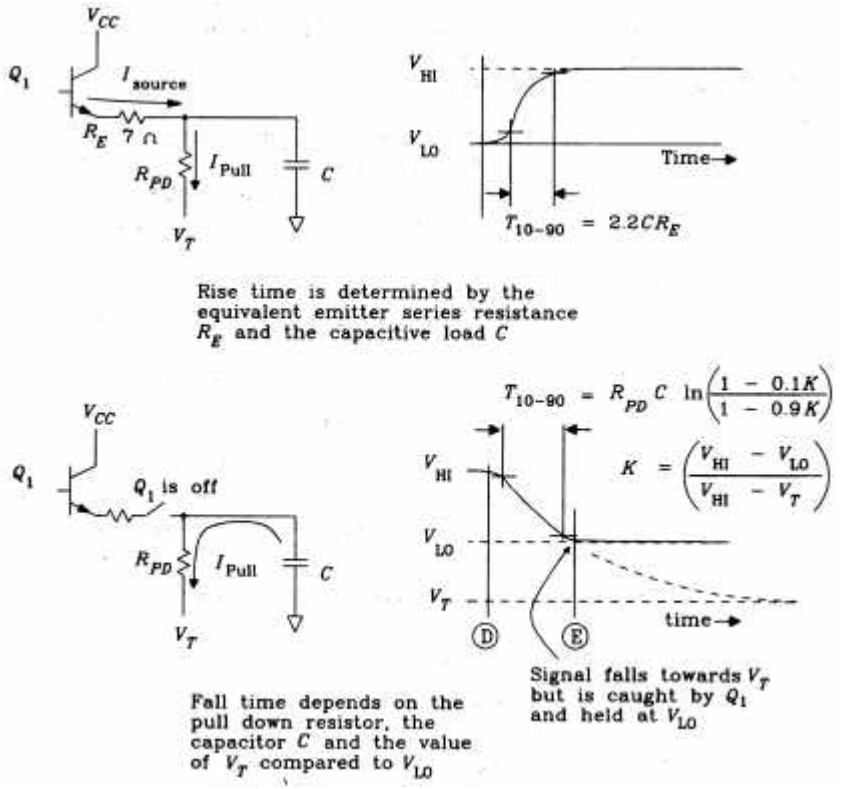
Quiescient Power in CMOS Totem-pole output circuit



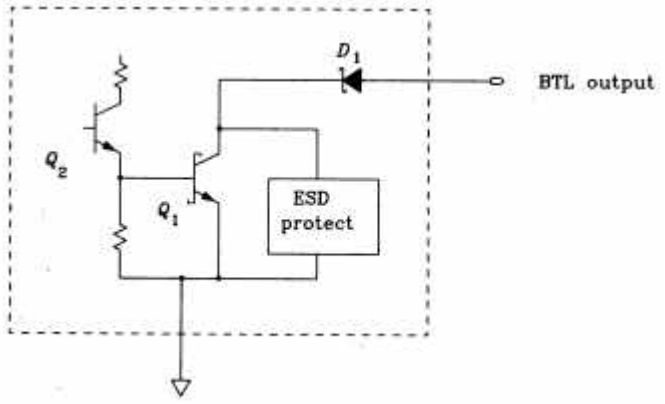
Active Power in Totem-pole output circuit



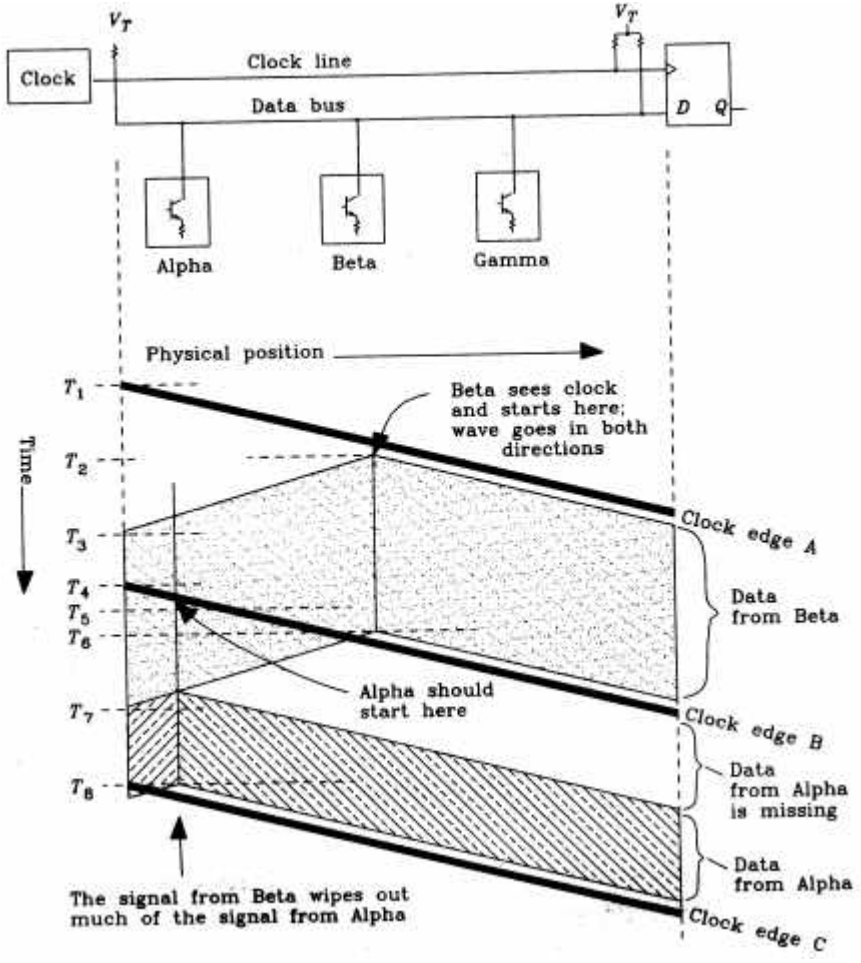
Rise and Fall times in Emitter follower circuit



BTL Output



Current source drivers



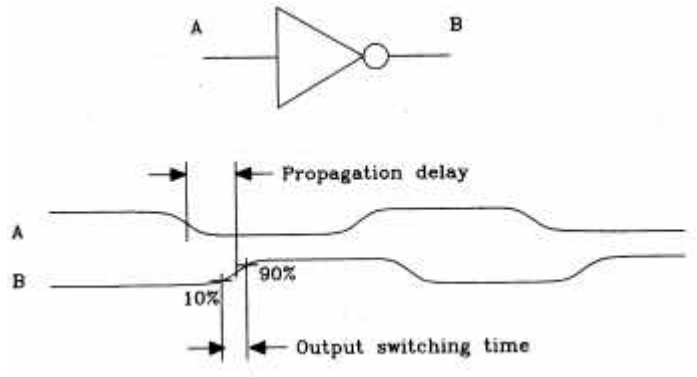
Output Dissipation

- Power supply - Terminating resistors, pull-down resistors, or other bias resistors

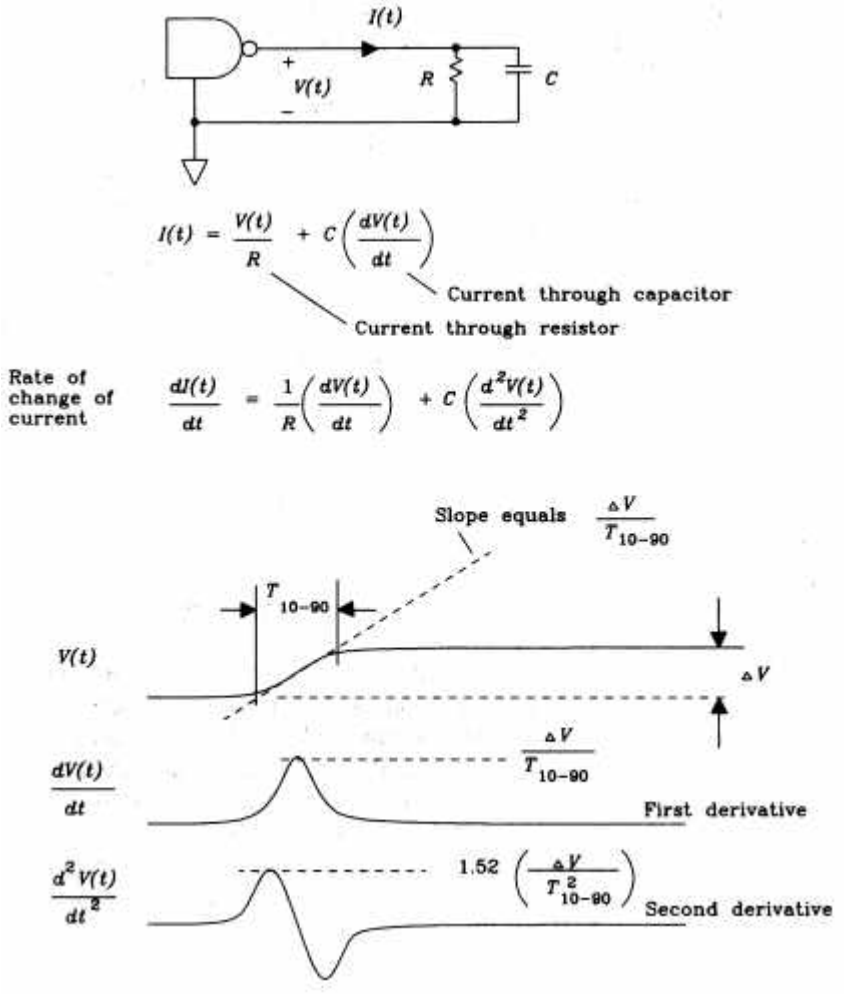
Speed

- Effects of sudden change in voltage,dV/dt
- Effects of sudden change in current,dI/dt

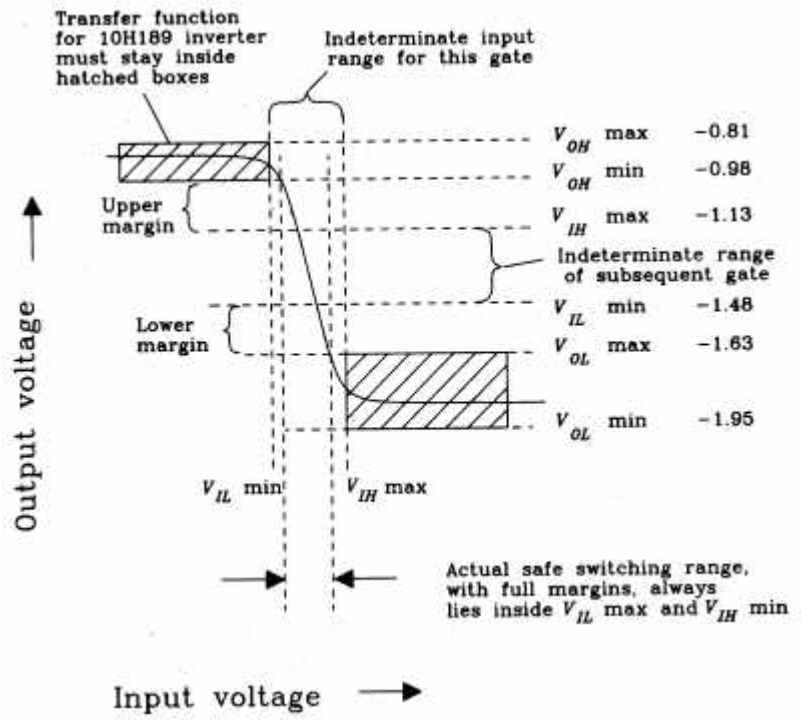
Output switching time Vs Propagation delay



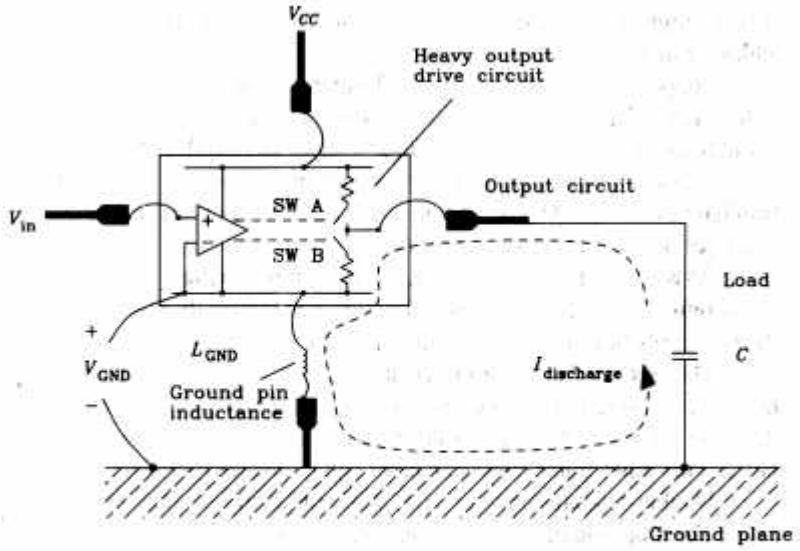
Max current slew rate Vs Voltage Rise time



DC Voltage margins for 10KH ECL

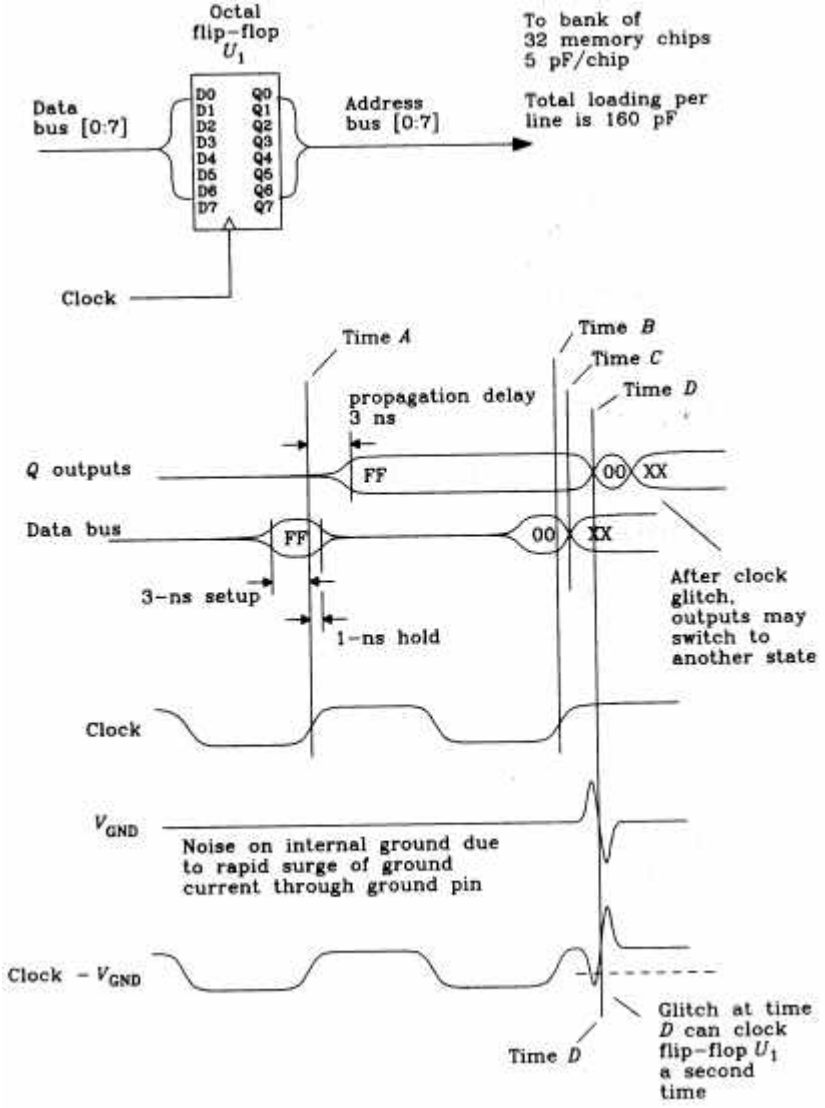


Ground Bounce - Lead Inductance

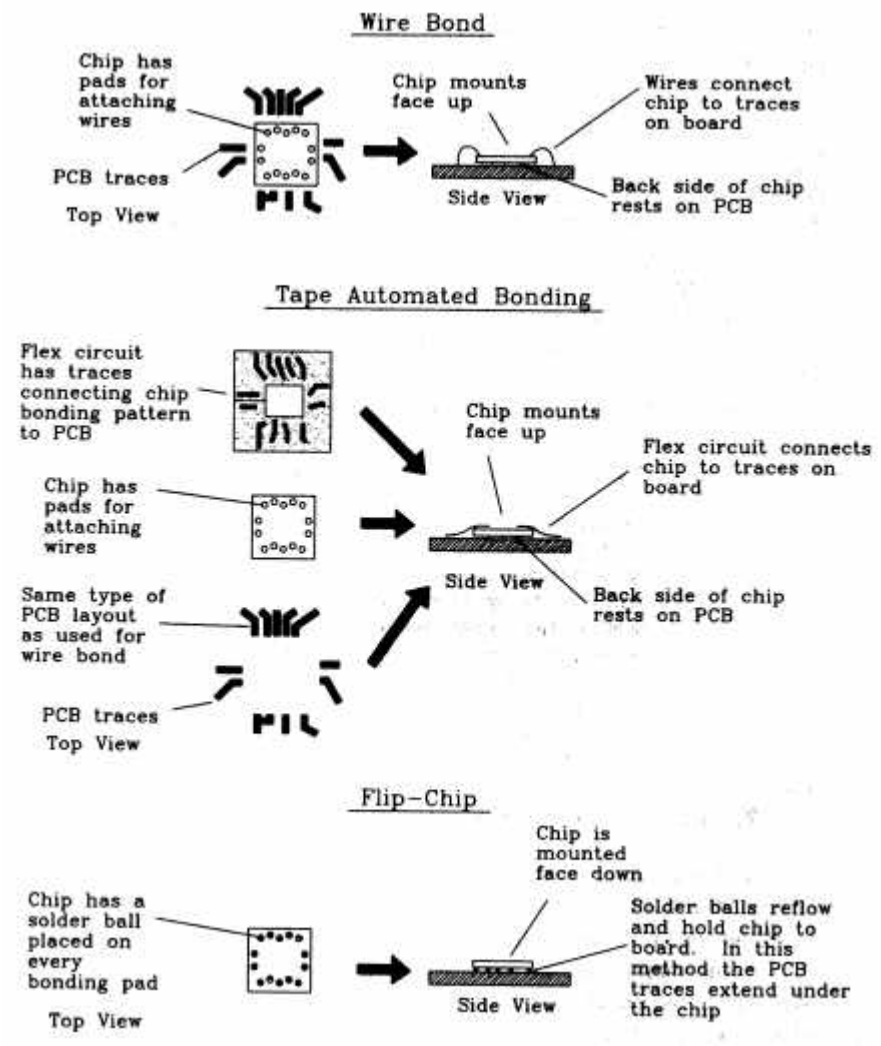


$$V_{GND} = L_{GND} \frac{d}{dt}\left(I_{discharge}\right)$$

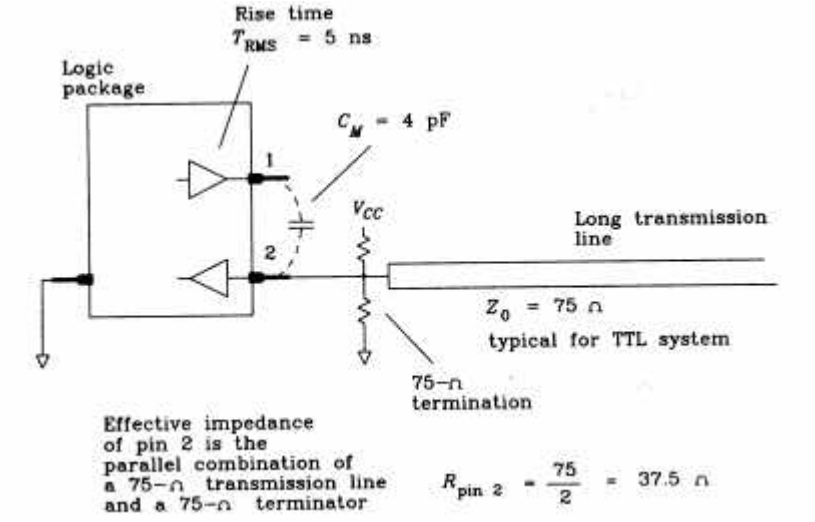
Ground bounce an example



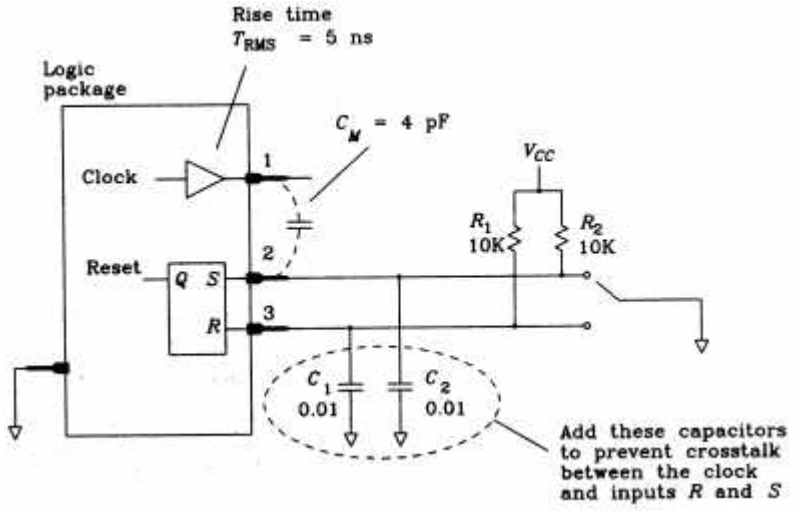
Packages


Wire Bond
Chip has pads for attaching wires
PCB traces
Top View
Chip mounts face up
Wires connect chip to traces on board
Side View
Back side of chip rests on PCB
Tape Automated Bonding
Flex circuit has traces connecting chip bonding pattern to PCB
Chip has pads for attaching wires
Same type of PCB layout as used for wire bond
PCB traces
Top View
Chip mounts face up
Flex circuit connects chip to traces on board
Side View
Back side of chip rests on PCB
Flip-Chip
Chip has a solder ball placed on every bonding pad
Top View
Chip is mounted face down
Solder balls reflow and hold chip to board. In this method the PCB traces extend under the chip
Side View

Lead Capacitance



Stray capacitance problem in a debouncing circuit

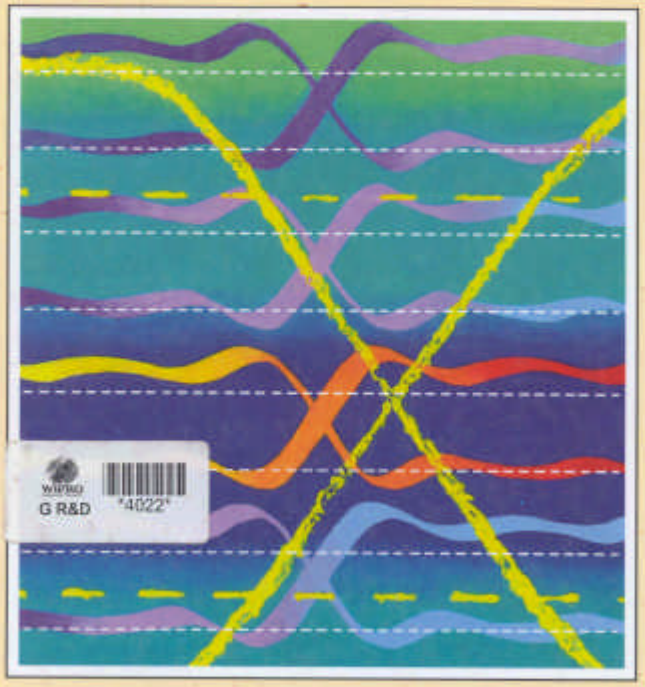


References

- “High- Speed Digital Design - A Handbook of Black Magic”, Howard Johnson, Martin Graham, Printice Hall PTR, 1993

HIGH-SPEED DIGITAL DESIGN

A HANDBOOK OF BLACK MAGIC



Howard Johnson
Martin Graham