A Compact Folded-cascode Operational Amplifier with Class-AB Output Stage

EEE 523 Advanced Analog Integrated Circuits Project Report

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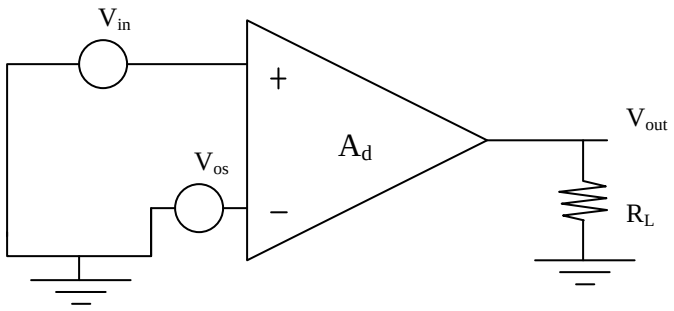
You are an engineer who is assigned the project to design a new CMOS high-gain operational amplifier uP523. The market for the uP523 is to be low power applications, such as hearing aids, heart pacemakers, etc. Since these applications are battery powered, the power supplies will be 5V. The performance objectives are listed below; note that the amplifier has only a single-ended output.



SPECIFICATIONS
An amplifier is to be realized that meets the following specifications:

1. A differential to single-ended voltage gain $A_d > 60{,}000$
2. An output voltage swing: >3V peak-to-peak driving $R_L = 1k\Omega$.
3. A unity gain bandwidth $f_u > 50MHz$.
4. The input offset voltage *Vos* must satisfy $Vos \cdot A_d < 20mV$ for your value of A_d.
5. DC power dissipation and chip area should be minimized.
6. Phase margin $PM > 60^o$
7. You can use only one voltage source V_{dd} (5V) for your circuit

Device Models:

- Use the MOSIS AMI 0.6um technology
- Assume this is an n-well process. Also, you can tie the well (body) of the PMOS device to the source.
- Nominal temperature $T = 25^0C$.

1. Opamp topology

The gain and bandwidth requirements of the amplifier are quite high. Gain is about 95 dB while the bandwidth is about 50M Hz. The load of the amplifier is resistive: Rl=1K Ohms.

We choose the topology shown in Figure 1. It is a folded-cascoded OTA with a calss-AB output stage. The folded-cascoded OTA provides a very good gain-signal swing trade-off. The OTA is a one-stage amplifier with quite large gain, so it is relative easy to design and to be compensated. The disadvantage of the OTA is that it can not drive resistive load. So we add the OTA with a class-AB output stage. Compare to class-A, class-B output stages, class-AB provide a good trade-off between power consumption and distortion.

Because the overall amplifier has a two stage structure, stability could be a problem. Here we use the cascode miller compensation technique to do the compensation. Compared to simple miller compensation, the cascode topology provides better PSRR and stability [1,2,3]. Note that M8a,9a and M8b,9b in Figure 1 form the floating current source to bias the class-AB output stage [2,3].

The folded-cascoded OTA uses the wide-swing cascode structure to provide better output signal swing. This wide swing structure needs wide swing bias circuitry, which is shown in Figure 2. The bias current I_b in Figure 2 is produced by a constant-gm bias circuitry [4], as shown in Figure 3. The constant-gm bias circuit needs a start-up circuit, which is not shown in the figure. In order to bias the wide-swing cascode structure properly, the transistors in the bias circuitry should be sized correctly. The transistor size in Figure 2 is only one option which the author to choose. Detailed sizing technique can be found in [4]. Figure 3 is the detailed bias circuitry used in this project, due to some matching considerations, more transistors are used in the real circuit than the simple one shown in Figure 2. But the simple one shown in Figure 2 should work fine.

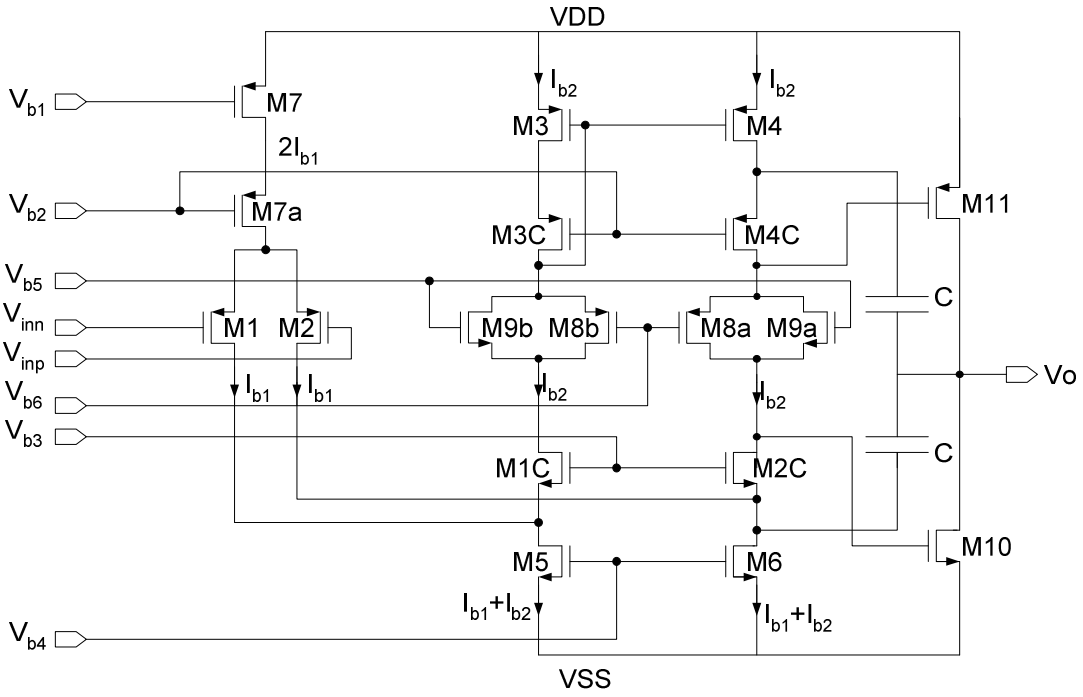


Figure 1 A folded-cascoded OTA with class-AB output stage.

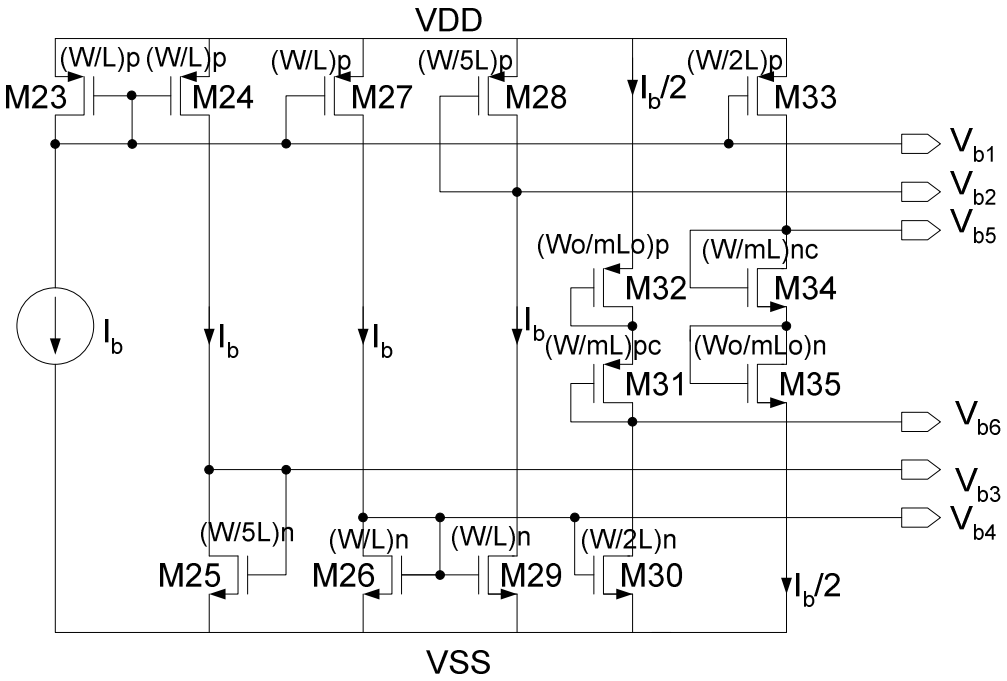


Figure 2 Simple bias circuit for the folded-cascoded OTA with class-AB output stage.

2. Detailed design procedure and hand calculations

The low frequency gain of the first stage, the folded-cascode OTA, can be written as:

$$A_1 = g_{mi} \times r_o \quad \text{(Equation 1)}$$

where g_{mi} is the transconductance of the input transistor M1 and M2, and r_o is the output impedance seen at the output of the OTA. One way to increase the gain is to increase g_{mi}, which can be done by increase their bias current, I_{b1} in Figure 1, and/or their aspect ratio $(W/L)_{1,2}$. Note that g_{mi} is proportional to the square root of both I_{b1} and $(W/L)_{1,2}$, which indicates this is not very efficient methods. In this design, in order to achieve large g_{mi}, minimum channel length, 0.6um for this process, is used for M1 and M2.

The output impedance r_o can be written as:

$$r_o = [g_{m3c} r_{o3c} r_{o3}] \| [g_{m1c} r_{o1c} (r_{o5} \| r_{o1})] \quad \text{(Equation 2)}$$

One efficient way to increase r_o, hence the gain of the OTA, is to decrease the bias current I_{b2}. Note that both g_{m1c} and g_{m3c} are generated from I_{b2}. Assume that:

$$g_{m3c} r_{o3c} r_{o3} = g_{m1c} r_{o1c} (r_{o5} \| r_{o1}) \quad \text{(Equation 3)}$$

We simply represent r_o as:

$$r_o = \frac{1}{2} g_{m3c} {r_{o3c}}^2 \quad \text{(Equation 4)}$$

We know that:

$$g_{m3c} \propto \sqrt{I_{b2}} \quad \text{(Equation 5)}$$

and

$$r_{o3c} \propto \frac{1}{\lambda I_{b2}} \quad \text{(Equation 6)}$$

Where:

$$\lambda = \frac{Kds}{2L\sqrt{V_{DS} - V_{eff} + \Phi_0}} \quad \text{(Equation 7)}$$

More detailed explanations on the above two equations can be found at [4]. We finally can find that:

$$r_o \propto \frac{1}{I_{b2}^{3/2}} \quad \text{(Equation 8)}$$

Which indicate decreasing I_{b2} can increase r_o, and hence the OTA gain.

The decrease of I_{b2} can be tricky. If not be careful, systematic offset can be introduced. The requirement of no systematic offset is that the drain current of M5 is equal to the sum of I_{b1} and I_{b2}. So the size of M3,4, M3c,4c, M1c,2c, M5,6 should be set in proportional to their drain current, so that their *drain current density* is equal to their corresponding parts in the bias circuitry. Note that if I_{b2} is very small, matching could be an issue. Another issue for small I_{b2} is the slew rate. So there is a trade off between gain and offset, slew rate. A common practice, used by textbook and many engineers, is $I_{b1}=I_{b2}$ [3]. In this design, we set $I_{b1}=4I_{b2}=240$uA. Compared to the normal setting $I_{b1}=I_{b2}=240$uA, we get about 6 dB extra gain, in addition to saving of power and area.

The gain of the second stage, the class-AB output stage, can be written as:

$$A_2 = (g_{m10} + g_{m11})(r_{o10} \parallel r_{o11}) = g_{m10} r_{o10} \quad \text{(Equation 9)}$$

Where we assume $g_{m10}=g_{m11}$ and $r_{o10}=r_{o11}$. It is also helpful to note that decreasing the bias current of the second stage increase its gain too. Its bias current is determined by the size ration between M10 and M34 (M34 is in Figure 2), M11 and M32. Detailed explanations can be found at [2,3].

Now we do some hand calculations on unit-gain bandwidth. For the process we used for this design, we know for NMOS: K'n=(Uo*Cox/2)= 56.0 uA/V^2, for PMOS, K'p= -16.2 uA/V^2 [5]. For $I_{b1}=240$uA, we have:

$$g_{m1} = \sqrt{2\mu_p C_{ox}(W/L)I_D} = \sqrt{4\times 16\times 10^{-6}\times\left(\frac{200}{0.6}\right)\times 300\times 10^{-6}} = 2..26 mA/V \quad \text{(Equation 10)}$$

For a compensation capacitor of 4pF, resulting in a unit-gain bandwidth of:

$$f_u = \frac{g_{m1}}{2\pi Cc} = \frac{2.26\times 10^{-3}}{2\pi\times 4\times 10^{-12}} = 90\ \text{MHz} \quad \text{(Equation 11)}$$

The required output swing is 3V. In this design, the output stage is a push-pull stage which can swing to both power supply rails. To drive a resistive load Rl=1K Ohm, the maximum source or sink current provided by the output stage is given by:

$$I_{\text{sink}} = I_{source} = \frac{Vswing}{Rl} = \frac{5}{1000} = 5\,\text{mA} \qquad \text{(Equation 12)}$$

This value determines the minimum size of the output stage.

3. Final schematics and simulation results

In the previous section, we presented the overall considerations and some design target value. In this section we present the final design results. The detailed bias circuitry and opamp are shown in Figure 3 and Figure 4 respectively.

Table 1 shows the summary of this design.

The simulated GBW is 58M Hz (see Figure 5). Compared to calculated value of 90M Hz. the simulated value is smaller, which may be due to the short channel effect so that gmi is smaller that the value calculated using square law. Also the actual value of Cc is larger because of the parasitic capacitance.

The output stage steady state current is about 2.5 mA. This value should be mc time the value of the floating current bias M31, M32 and M34, M35 (Figure 2). With mc=40, this value is 62 uA. The simulated value is 42 uA. Note the AC current of the output stage could be much larger than its steady state value of 2.5mA. So that required value of 5mA should be able to easily achieve.

We use the bias technique of $I_{b1}=4I_{b2}$ to increase the gain. This also achieve small area and low power compared to conventional $I_{b1}=I_{b2}$ bias.

Simulation shows that the first folded-cascode stage has a gain of 66 dB which the second stage has a gain of about 30 dB.

Because we use a push-pull output stage, the output voltage swing is rail to rail. Figure 6 shows the simulation results. It can be seen that the output swing is rail-to-rail. Also from the figure we can find about 85 uV input offset. Another results we can get from this figure is that the gain=ΔVout/ΔVin is roughly 60,000.

Figure 7 shows the transient response with a step input of the opamp in the unit-gain configuration. It can be seen that the opamp is stable. From this figure we can find the slew rate of the opamp is about 77V/uS. We know I_{b2}=77uA (see Figure 9), and C=2pF. Then the slew rate can be calculated as:

$$SR = \frac{2I_{b2}}{C} = 77V/uS \qquad \text{(Equation 13)}$$

which is in a very good agreement with simulation result.

Figure 8 shows the input-common model voltage range and the output voltage swing.

Figure 9 shows the DC operating points and DC node voltage of the opamp. Every transistor is saturation mode, as designed.

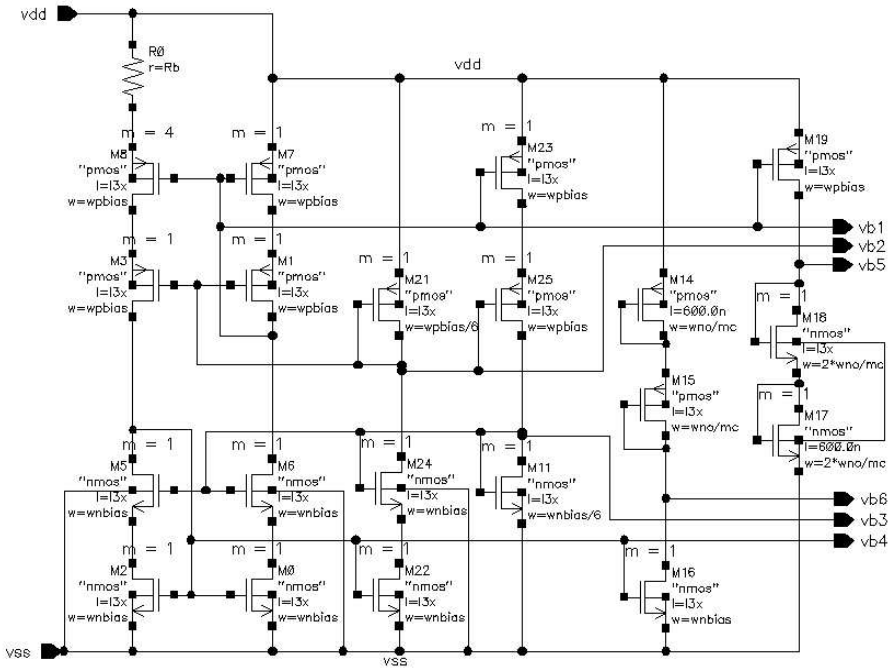


Figure 3 Detailed bias circuit (without start-up circuit)

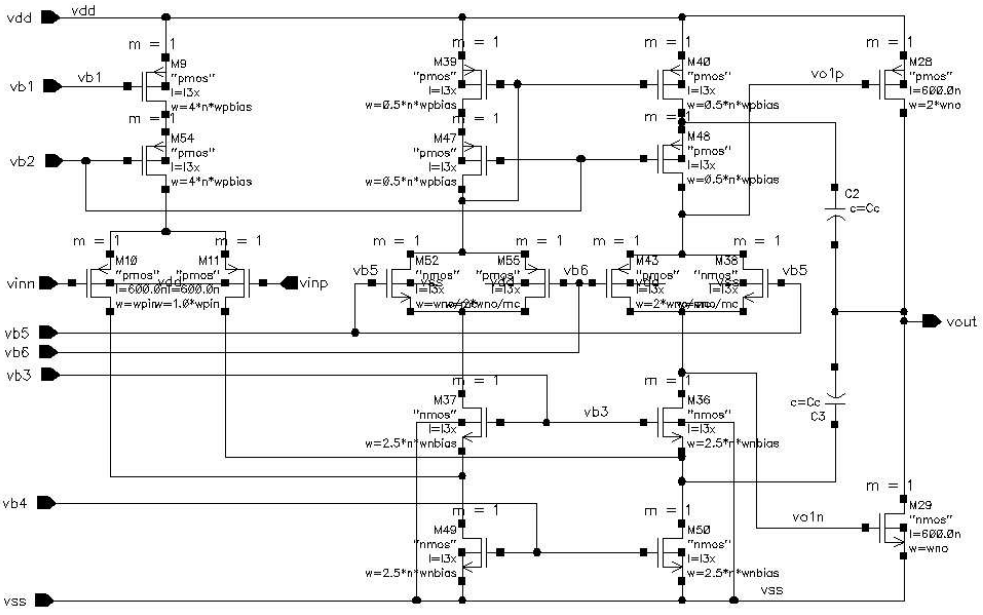


Figure 4 Detailed schematic used in this project

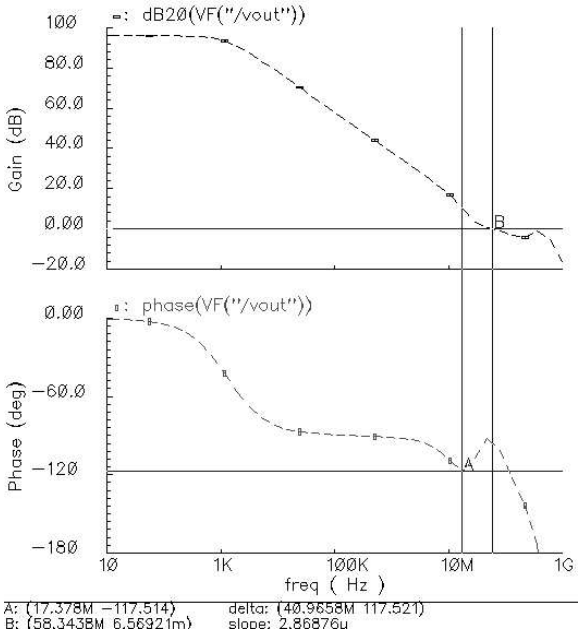


Figure 5 Simulated gain and phase of the opamp.

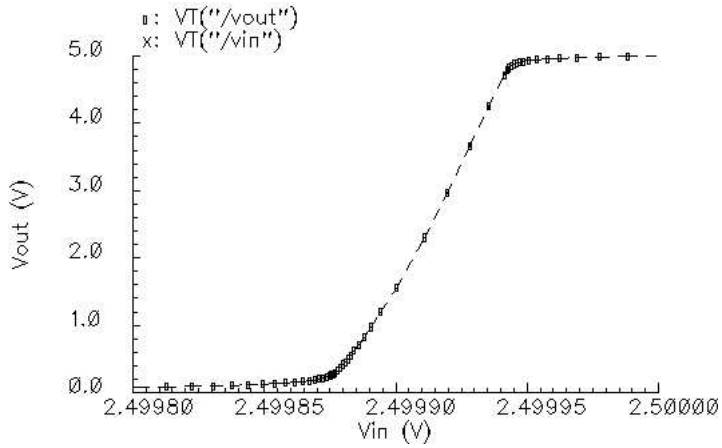


Figure 6 Vout Vs Vin, Vinn=2.5V. Slowly sweep winp from 2.499 to 2.501V. About 85 uV input offset is shown.

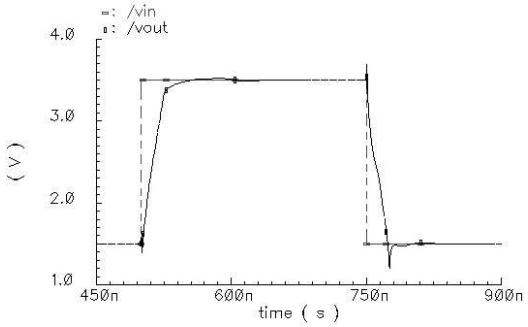
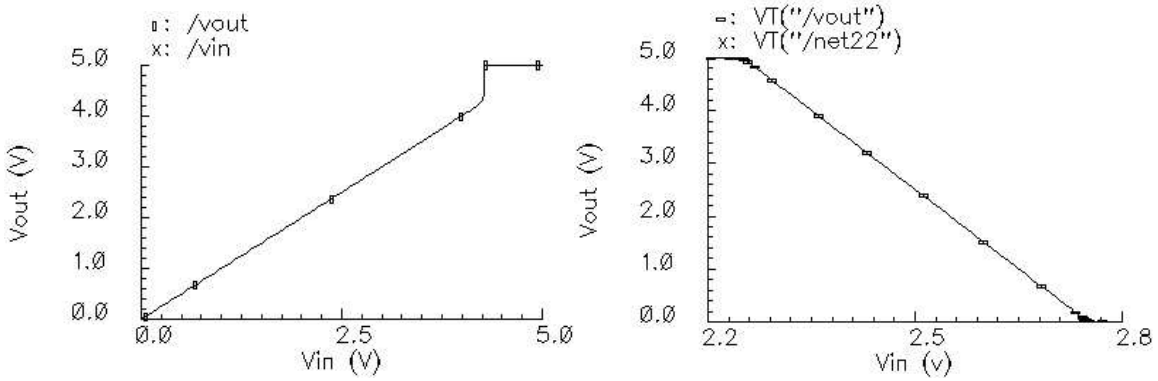


Figure 7 Step response of the opamp as a unit-gain buffer.



(a) (b)

Figure 8 (a) Input common-mode voltage range simulated with a unit-gain buffer configuration. (b) Output voltage swing simulated using a inverting gain of 10 configuration [6].

Table 1 Design Summary

Name	**Simulated Value**	**Design Value**	**Comment**
Rb	3K Ohms	3K Ohms	Constant-gm bias
Cc	2p F	2p F	Compensation capacitor
mc	40		Ratio of channel width, mc=W_{11}/W_{32}= W_{10}/W_{35}
I_{b1}	234 uA	300 uA	See Figure 1
I_{b2}	77 uA	100 uA	Design value: I_{b1}/ I_{b2}=4
L3x	3.0 um	2.0 um	Channel length of all devices except input and output stages.
Lmin	0.6 um	0.6 um	Channel length of input/output stage M1, M2, M10 and M11.
Wpin	200 um	200 um	Input transistor M1, M2 channel width
Wno	800 um	800 um	Output NMOS transistor M10 channel width
Wpo	1600 um	1600 um	Output PMOS transistor M11 channel width
n	3	4	Channel width ratio. See Figure 4.
Gain	96 dB	96 dB	DC gain
GBW	58M Hz	50M Hz	Unit gain bandwidth
Iamp	3.2 mA	N/A	Total DC current consumption of the opamp
Ibias	240 uA	N/A	Total DC current consumption of the bias circuitry
Vosw	5 V	5V	Output voltage swing
CMR	0-4V	N/A	Input common mode voltage range
SR	77V/uS	N/A	Slew Rate
Vos	90uV	<20 mV/Ad	Input offset

4 Conclusion and discussions

In this project, we successfully designed an opamp with a low frequency gain of 96 dB and unit-gain bandwidth of 50MHz, with a resistive load of 1K Ohm. It is a high potable, robust design, very insensitive to process, voltage and temperature variations. The first stage is a folded-cascode OTA biased in the wide-swing configuration, with a gain of about 66 dB. The second stage is a class-AB output stage, with a gain of 30 dB. The steady stage current of the second stage is controlled by a floating current source. With a single 5 V power supply, the input common mode range is about 4 V and the output voltage is rail-to-rail. In order to enhance OTA gain, some new bias techniques were used. The input offset voltage is a little bit large. In the application, this input referred offset can be reduced by auto-zero or chopper techniques.

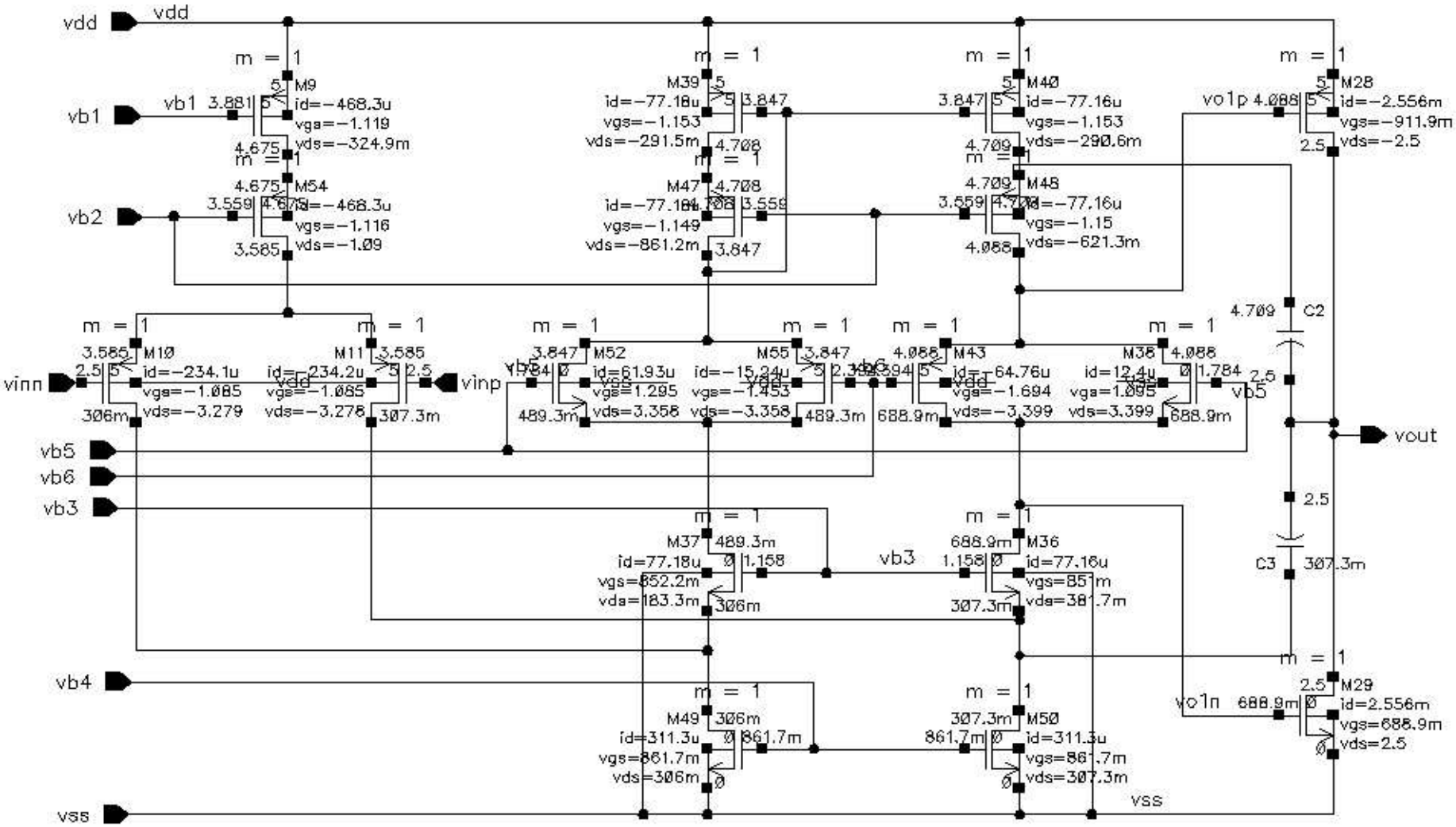


Figure 9 DC operating points and DC node voltage

Reference

[1] B.K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 18(6), pp.629-633, Dec. 1983.

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[3] Roubik Gregorian, *Introduction to CMOS Op-amp and Comparators*. New York: Wiley, 1999

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[5] MOSIS webpage http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/n8bn-params.txt.

[6] P.E. Allen, D.R. Holberg, *CMOS Analog Circuit Design*, Nre York: Oxford, 1987