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Optimization of PLL and Serializer

Master of Science Thesis

By

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Stockholm, 2001

Master of Science (*Teknologie Magister*) Thesis
in *System-on-Chip Design*

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Abstract

The progress in CMOS sub-micron technology has enabled designers to easily integrate complex digital and mixed signal systems on the same die. As a consequence integrated systems are now more powerful and operate at higher speed than previous devices. Meanwhile, as the speed of the integrated circuits (ICs) is increased, classical techniques and circuits used efficiently at low speed have to be replaced by new and faster ones. One of the important circuits used in modern ICs is the phase locked-loop (PLL) and serializer.

The phase-locked loop is a non linear circuit and its design and optimization involves many trade-offs. Usually, the PLL bandwidth and cut-off frequency should not be too large in order to specify noise and stability and speed requirements. PLLs superior immunity and tracking capability makes it very attractive in many applications, e.g. clock distributions, clock-recovery, bit synchronization, frequency synthesis, and demodulation. A special type of PLL is the charge-pump PLL, which has the advantage of an extended frequency range of operation and low-cost. While the serializer is used for the data translation between the serial bits and the parallel bytes.

In this project, the design and layout techniques used to implement the different components of PLL are being discussed. Also the full custom layout design of complex digital serializer for high speed applications has been implemented as a separate project. The chip will be fabricated using Infineon C10- $0.18\mu m$ CMOS process, having six layers.

Keywords

PLL, Charge Pump, Phase/Frequency detector, VCO, feedback, Serializers, Clock, Layout techniques, C10-0.18µm CMOS technology.

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