

Optimization of PLL and Serializer

Master of Science Thesis

By

Yaseer Arafat Durrani

Stockholm, March 2002

Supervisors: Dr. Tim Koerner and Rashid Malik at Infineon Technologies AG, Berlin, Germany

Supervisors: LiLi at IMIT/KTH

Examiner: Dr. Hannu Tenhunen at IMIT/KTH



ROYAL INSTITUTE OF TECHNOLOGY

Optimization of PLL and Serializer

Yaseer Arafat Durrani

Stockholm, 2001

Master of Science (*Teknologie Magister*) Thesis
in *System-on-Chip Design*

Supervisors:

Dr. Tim Kronor
MSc. Rashid Malik

Examiner

Dr. Hannu Tenhunen(KTH)

Supervisor

Researcher LiLi

Infineon Technologies AG

Optic Fiber Department
Berlin, Germany

Royal Institute Of Technology (KTH)

ESDLab, Department of Microelectronics
and Information Technology
Stockholm, Sweden

Optimization of PLL and Serializer

Yaseer Arafat Durrani

*Master of Science in System on a chip Design
Department of Microelectronics and information technology
Royal Institute of technology (KTH), Sweden*

Done at
Infineon Technologies AG, Berlin, Germany

Abstract

The progress in CMOS sub-micron technology has enabled designers to easily integrate complex digital and mixed signal systems on the same die. As a consequence integrated systems are now more powerful and operate at higher speed than previous devices. Meanwhile, as the speed of the integrated circuits (ICs) is increased, classical techniques and circuits used efficiently at low speed have to be replaced by new and faster ones. One of the important circuits used in modern ICs is the phase locked-loop (PLL) and serializer.

The phase-locked loop is a non linear circuit and its design and optimization involves many trade-offs. Usually, the PLL bandwidth and cut-off frequency should not be too large in order to specify noise and stability and speed requirements. PLLs superior immunity and tracking capability makes it very attractive in many applications, e.g. clock distributions, clock-recovery, bit synchronization, frequency synthesis, and demodulation. A special type of PLL is the charge-pump PLL, which has the advantage of an extended frequency range of operation and low-cost. While the serializer is used for the data translation between the serial bits and the parallel bytes.

In this project, the design and layout techniques used to implement the different components of PLL are being discussed. Also the full custom layout design of complex digital serializer for high speed applications has been implemented as a separate project. The chip will be fabricated using Infineon C10-0.18 μ m CMOS process, having six layers.

Keywords

PLL, Charge Pump, Phase/Frequency detector, VCO, feedback, Serializers, Clock, Layout techniques, C10-0.18 μ m CMOS technology.

Acknowledgment

First of all I would like to thank my Allah Almighty for giving me strength.

I would like to thank Dr. Hannu Tenhunen for giving me admission in the System-on-chip (SoC) design program. Also I would like to thank Prof. Elena Dubrova, who is the co-ordinator of the SoC program. I would also like to thank my KTH supervisor LiLi, who encouraged me in my thesis and study work.

I am greatly indebted to Karl Schrödinger, Manager development department, Optic Fiber for giving me the opportunity to do my thesis at Infineon Technologies AG, Berlin, Germany. I am very thankful for his help and motivation during my thesis period. My sincere gratitude to my supervisors Dr. Tim Koerner and Rashid Malik, in Infineon Technologies AG for their kind and sincere help and guidance throughout the thesis period. I would also like to thank them for spending their time in my project and explaining many things I hadn't known before, inspite of their busy schedule.

My sincere thanks to all my SoC classmates, those near and dear for all the kindness, advice and friendship. On the personal front, my love to my parents and brothers/sister for encouraging me all through my life.

Yaseer Arafat Durrani
SoC Masters,
March, 2002
Stockholm, Sweden.

Table of Contents

1.Introduction.....	01
1.1 Background & objective.....	01
1.2 Thesis Organization.....	02
2. PLL Architecture.....	03
2.1 Basic PLL Loop Architecture.....	03
2.2 Basic PLL Topology.....	04
2.2.1 PLL Waveforms in Locked Condition.....	05
2.2.2 Small Transients in Locked Conditions.....	06
2.3 Phase Lock Loop Stability Analysis	07
2.3.1 PLL response with no loop filter.....	09
2.3.2 PLL response with open loop filter.....	10
2.3.3 PLL response with a pole-zero loop filter.....	13
3. Charge-pump and Phase/Frequency Detector.....	15
3.1 PLL with Charge-Pump Phase Comparators.....	15
3.2 Phase/Frequency Detector.....	15
3.3 Charge Pump.....	17
3.3.1 Basic Charge-Pump PLL Principle.....	18
3.3.2 Dynamic of CPPLL.....	20
3.4 Nonideal Effects in PLLs.....	22
3.5 Jitter in PLL.....	25
4.Loop Filter	27
4.1 Capacitor.....	27
4.2 MOS capacitor characteristics.....	27
4.3 Capacitor measurements.....	28
4.4 P-MOS capacitors.....	28
4.5 The RC circuit.....	29
4.6 The advantages and disadvantages of RC circuit.....	32
5.Serializer	33
5.1 Significance of the Serial Communication Device.....	33
5.2 Functional Overview of the Serialicom Devices.....	33
5.3 Serializer & Clock generator.....	34
5.4 Ethernet Network Elements.....	35
6.CMOS Layout Considerations.	36
6.1 Infineon C10-0.18micron Technology.....	36
6.2 The design rules.....	36
6.3 General layout guidelines.....	37
6.4 CMOS standard cell design.....	37
6.5 Cell placement techniques.....	39

6.5.1 Planning.....	39
6.5.2 Style.....	40
6.6 Power and Ground Connections.....	42
6.7 Wire length design.....	44
6.8 CMOS gate transistor sizing.....	44
6.9 Routing Capacitance.....	45
6.10 Distributed RC effects.....	45
6.11 Performance.....	45
6.12 Cell speed.....	45
6.13 Interconnect speed.....	46
6.14 Gate Optimization.....	46
6.15 Clock Distribution.....	47
6.15.1 Placement.....	47
6.15.2 Routing.....	47
7.Conclusion.....	48
8.Bibliography.....	49
9.Appendix.....	51