Hemant Savla

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OBJECTIVE

Seeking a full time position in Electrical Engineering.

Area of Interest :- *RF / Analog / Digital Circuit Design, ASIC /RTL design and Testing, Computer-Architecture*

EDUCATION

- **M.S.,** *Electrical and Computer Engineering* (Dec 2003)
  University of Wisconsin-Madison, WI (GPA = 3.74/4.0)
  Advisor: - Prof. Charlie Chung-Ping Chen
  Thesis:- The Design of a Low Power Bluetooth Transceiver
  Relevant Course Work : -
  - Advanced Computer Architecture
  - VLSI System Design
  - FPGA Design Laboratory.
  - Advanced Topics in Digital System Testing
  - Analog CMOS Integrated Circuit Design
  - Applied Communications Systems
  - Advanced Communication Circuit Design

- **B.E.,** *Electronics Engineering* (Jan 2001)
  Sardar Patel University, India (GPA = 9.42/10, ranked 1st in a class of 68 students)
  Relevant Course work: -
  Embedded System Design and Programming, Digital Signal Processing, Process Control Engineering and Power Electronics.

WORK EXPERIENCE

Research Assistant July 2002 – Jan 2004
VLSI-EDA Group, University of Wisconsin-Madison, WI
- Led a design effort to implement a low power RF/Analog transceiver for **Bluetooth** technology in TSMC 0.18µm CMOS technology. [http://vlsi.ece.wisc.edu/Projects.htm]

Design Engineer Jan 2001 – Dec 2001
Chain Electronics Pvt. Ltd., Gandhinagar, India
- Developed a CNC Drilling Machine capable of drilling 56 holes/second in Printed Circuit Boards.
- Designed a low cost Copper Thickness Measuring Meter to measure the thickness of copper foil laminated on the base material of Printed Circuit Boards.
- Supervised the designing and manufacturing of Flexible Printed Circuit Boards

Summer Intern May 2000 – July 2000
Multispan Instruments Company, Ahmedabad, India
- Developed an In Circuit Programmable digital temperature controller board with Atmel's RISC Controller AVR.

ANALOG / RF DESIGN PROJECTS

RF/Analog Bluetooth Transceiver in TSMC 0.18µ CMOS technology.
- Designed, simulated and layout of LNA, Mixer, OTA-C Filter, Demodulator, Sigma-Delta DAC, VCO, a Phase Locked Loop (PLL), using Cadence and Agilent's ADS software.
- Designed receiver achieves a sensitivity of -80 dBm.

Analog Multiplier and OpAmp Design

- Design & Implementation Analog Multiplier and OpAmp in 0.5µm CMOS technology using Tanner Tools. An OpAmp with gain of 75dB and a bandwidth of 250Mhz was designed.

Low Noise Amplifier (LNA) for Bluetooth Transceiver

- LNA provides a gain of 12 dB, for a noise figure (NF) of 2.84dB and an input referred IP3 of +7.39 dBm.

Microstrip Patch Antenna for a 2.4GHz ISM band Transceiver

- Designed the antenna and developed a setup for antenna pattern measurement in an anechoic chamber.

ASIC / DIGITAL CIRCUIT DESIGN PROJECTS

3D Graphics Processing Unit (GPU)

- Led a team of 4 people in implementing a 3D Graphics Processing Unit (GPU) on Xilinx XSV-800 FPGA operating at 12.5 MHz with a resolution of 256 x 480.
- A *16 bit Float Point 5 stage Pipelined RISC Processor* capable of processing more than 1000 vertices/second and a *Rasterizer pipeline* having a throughput close to 1 pixel / clock cycle were designed. 34% FPGA resource usage

3D Graphics support for PLX Processor

- Adding various float point instruction to **PLX Processor** (a subword parallel processor) for 3D graphics capabilities. Designed hardware to support float point ADD, multiply, MAC, LOG, reciprocal and reciprocal square-root.

Programmable Digital Filter

- Transistor level design, simulation and layout (in 0.35µm technology) of a 4-Stage Pipelined Programmable Digital Filter with a throughput of 166Msamples/s using Mentor graphics and simulation with Eldo (a spice simulator) shows that the system meets the constraints like delay and area.

Digital Circuit Testing: -

- Developed an efficient test set for a circuit of approx 10,000 gates capable of not only detecting the stuck at faults but also pinpointing the locations of those faults in circuit using Perl scripts.

COMPUTER SKILLS

CAD Tools

- Extensive experience with
  - Mentor Graphics IC design flow (Design Architect, IC station, Calibre, Eldo, Quicksim) and
  - Cadence IC design flow (Virtuoso, Diva, Assura, Spectre-RF, Verilog-NC, Virtuoso-XL).
- Extensive experience with Agilent's ADS, Tanner Tools (L-Edit & T-Spice), Hspice, Matlab, Xilinx foundation, FPGA express, ModelSim, Synopsys' Design Complier.

Languages

- Proficient in C/C++, Perl and Visual Basic programming
- VerilogHDL / VHDL / Verilog-A and 8051, 80x86, AVR, MIPS, 8085 Assembly language

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PUBLICATION

- *Hemant Savla, Sachin Garg, Vikas Sharma and Charlie Chung-Ping Chen* "A Low Power SoC for Bluetooth Transceiver in 0.18µm CMOS" **submitted for publication in Design Automation Conference (DAC), 2004.**

Reference available upon request