

Radio-Frequency Integrated Circuits for Portable Communications

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Introduction

While the greatest design efforts in silicon analog ICs have been historically aimed at baseband circuits, which range in frequency of operation from voiceband to communications circuits at tens of MHz, analog GaAs circuits have found a niche in microwave communications ICs by exploiting the high-frequency capabilities of the MESFETs and the semi-insulating properties of the substrate material to form on-chip inductors and transmission lines. These monolithic microwave ICs (MMICs) have enabled entirely new applications in the microwave and millimeter-wave ranges, from 10 GHz to beyond 100 GHz.

A new market has meanwhile emerged in the form of portable wireless communications devices, operating in the 900 MHz to 2 GHz range, where miniaturization and low-energy operation is sought through the aggressive large-scale integration typical of silicon ICs, yet the circuit design style at times resembles MMICs. Early indications suggest that silicon will be the technology of choice in this application, because analog and digital functions can freely intermingle on the IC, and because the transistor f_T both in production bipolar and CMOS technologies is adequate for operation in this range. Although there are only a few examples today of these "VLSI radios", they arouse much curiosity and speculation because it is anticipated that by the year 2000, close to 300 million of these consumer wireless devices will be in use [1].

This paper summarizes some of the key radio-frequency integrated circuit developments in the last thirty years, the majority of which have been developed for consumer use. From this survey, it projects what developments may be reasonably expected in the architectures and circuit blocks of RF ICs over the next five to ten years.

ICs in Broadcast Radio Receivers

Consumer electronics companies have been drawn, since the early days of IC technology, to the prospect of miniaturizing broadcast AM/FM receivers for use in the home, car, or even in the pocket. Following early efforts in the 1970's, AM/FM radios were reduced to either a single-chip containing functions from the IF amplifier onwards to the audio power amplifier [2], or to two- or three-chip sets [3, 4], surrounded by a dozen or more discrete filter modules, consisting of LC filters and, at high frequencies such as 10.7 MHz, ceramic resonator filters. ICs enabled unique solutions to some baseband functions, such as cheap phase-locked loops for the detection of pilot tones or for FM demodulation. In the front-end, the superior characteristics of the double balanced mixer using the four-quadrant analog multiplier could only be realized in IC form, while the RF tuned amplifiers and most of the inter-stage coupling elements remained discrete. However, ICs did not influence the architecture and frequency allocation plan in these receivers, which continued to resemble conventional discrete-component radios.

A re-thinking of the conventional FM receiver came about at Philips where Kasperkovitz [5, 6] realized that the main advantages of integration would come about by integrating the many filters on-chip, thus eliminating the multiple trims of the discrete filters in production. However, it was then impossible to integrate the RF or the 10.7 MHz IF bandpass filters on-chip either with spiral monolithic inductors or by simulating them electronically with gyrators. The key step in solving this problem was to lower the intermediate frequency from 10.7 MHz to 70 kHz. A small off-chip inductor provided some RF filtering, but the channel bandwidth was mainly defined on-chip by high-order active RC filters. The power dissipation in these filters for a given dynamic range scales down with the IF. This choice of IF also meant that the image frequency lies half way to the next FM channel (Fig. 1), so no special effort was required to suppress the image. As a consequence of the low IF, the received frequency deviation of ± 75 kHz was compressed to ± 15

kHz by a negative frequency feedback on a varactor-tuned VCO to avoid distortion caused by signal aliasing around DC. Integration also made it cost-effective to use a new muting system. This single-chip FM mono receiver [7] requires only 15 small capacitors and two inductors, making it possible to fit the entire system within a wristwatch. The 8 mA drain from a 4.5V supply made the bipolar IC attractive for use in miniature portable applications requiring a small battery volume.

The same idea of low IF has been pursued at Sony, seeking bipolar ICs operating at supplies as low as 0.95 V provided by a single battery [8]. It is likely that this research program has contributed to their now universally recognized product line of personal entertainment systems. Their latest FM radio IC is a double superheterodyne architecture. At 30 MHz, the first IF is high enough that a fixed bandpass filter in series with the antenna spanning the entire broadcast range from 80 to 110 MHz will substantially suppress the image signal; no on-chip filter is used. Then, a second mixer converts to a low IF of 150 kHz, and thereafter on-chip filtering is implemented by a 9th order active *RC* lowpass section. This IF is high enough to include the adjacent channel in the image, so an image rejection mixer (Fig.2) is used. This electronic solution to a difficult filtering problem was first described in the 1930's, but has only become practical on the IC. The image suppression is limited by matching in the two channels to 40 dB. An allpass active *RC-CR* filter produces quadrature phases of the local oscillator signal. This receiver drains about 15 mA in either FM or AM mode. The RF amplifier transistors are integrated on these ICs, although they require off-chip inductors for the load, and the local oscillator needs an off-chip *LC* tuned circuit.

ICs in Wireless Paging Receivers

The desirability of paging people on the move through a miniature wireless receiver was recognized in the early 1960s. The Bell System's Bellboy experiments [9] carried out in pre-IC days anticipated many of the key concepts that in later years were used in integrated paging receivers. The prototype system operated at 150 MHz, and frequency-modulated three tones on the carrier which the intended receiver could recognize by the simultaneous response of passive reed resonators. The receiver operated at 4 V using a total of only ten transistors [10]. The low IF of 6 kHz meant that simple capacitively-coupled 10 kHz *lowpass* (rather than bandpass) channel filters could be used, and that transistors after the RF section required

small bias currents. A cascode two-stage amplifier in the RF front-end re-uses the same bias current, a concept found even today in low-power MMICs.

Paging receivers have been in continuous development since, evolving into today's wide-area pagers with digital signalling. The modern pager signals anywhere from 500 to 1200 b/s by encoding data with a simple positive or negative offset of the carrier frequency — the binary frequency-shift keyed (FSK) modulation. Surprisingly, paging receivers up to the early 1980's did not exploit the powerful simplifications this signaling scheme implied, even though there was great market pressure to reduce the battery drain and miniaturize the receiver. A conventional double superheterodyne receiver of that era consisted of a first upconversion of the received signal to suppress the image channel with a crystal bandpass filter of modest complexity, and then a downconversion with further selection with a ceramic bandpass filter, followed by a frequency discriminator to demodulate the FSK [11]. Vance at Standard Telecommunication Laboratories realized how to simplify an FM receiver on to one chip with a quadrature downconversion mixer combined with zero IF. This was exactly the right solution for the binary FSK digital paging receiver [12]. This remarkably simple receiver (Fig.3) consists only of a quadrature demodulator, lowpass filters in each arm, limiters, and a D-type flip-flop detector, and when integrated on one bipolar chip, it drains 2.5 mA from 1.8 V when active, although in standby the drain falls to a mere 50 μ A. Large value off-chip capacitors were required for AC coupling and for the lowpass filters. A second low-frequency digital CMOS IC performed all the user interface functions. Zero IF meant that the mixer has *no* image, and because data is encoded in frequencies ± 4.5 kHz away from the carrier, DC offsets in the receiver or flicker noise below this frequency could be removed by capacitive coupling in the receiver. The 10 kHz lowpass filters serve to limit out of band noise and blocking signals from degrading the signal-to-noise ratio at the detector.

Pager ICs at Philips initially used a frequency-offset receiver principle [13], whereby the local oscillator frequency is offset from the received carrier by 2 kHz, thus converting the FSK tones to 2.5 kHz and (aliased to) 6.5 kHz. This requires a fairly sophisticated automatic frequency control, and a frequency discriminator to detect the data. Aside from the local oscillator crystal, three off-chip tuned circuits must also be provided. The tuned circuits are obviated in a zero-IF receiver [14], which

includes the filters on-chip. These consist of a third-order active *RC* lowpass filter, followed by a 7th order gyrator-based lowpass filter with a 15 kHz cutoff. The signal is amplified at these low frequencies. It is interesting to note that the only components on the front-end not integrated are the tuned load for the RF amplifier transistors, and the quadrature phase-shift network for the image reject downconversion; on this IC, both are combined in one off-chip signal path.

Others, too, have developed similar zero-IF bipolar integrated front-ends, sharing the feature that much of the die area is taken up by the capacitors for the on-chip lowpass filters [15, 16]. Zero IF and pager signalling were a perfect match, and the RF sections of the wireless paging receiver seems to have evolved little since Vance's work in 1982.

ICs in Cellular Telephone Transceivers

Mobile and handheld cellular telephones are the first widespread two-way radios for consumer use, for which cordless telephones were only a prelude. Radio telephones to be successful with consumers must meet stringent demands for low weight and volume, long battery life, and low cost. Further, to support a large numbers of users in a crowded radio spectrum, radio telephones require more signal processing than other common transceivers. They must therefore use higher levels of integration in the electronics.

The first ICs for use in portable communication devices contained the frequently occurring building blocks of conventional single or double superheterodyne receivers, such as the mixer and local oscillator, or the IF amplifier chain and signal-strength indicator [17]. These silicon ICs would typically be preceded by a discrete RF amplifier and a first mixer. The front-end components themselves, such as a tuned RF low-noise amplifier in the 900 MHz band, a mixer, and a local oscillator, were first integrated on GaAs ICs [18-21]. Aside from the superior high-frequency characteristics of the MESFETs, these ICs included spiral inductors as loads and as series feedback elements for low-noise input matching (Fig.4) [22]. It was by then well known after many years of GaAs MMIC development that the semi-insulating substrate and gold metallization were well-suited to the monolithic fabrication of large value inductors with a modest-Q and a high frequency of self-resonance. Other chip sets have addressed the frequency synthesizer and power amplifier control module [23], or

the downconversion and upconversion mixers for the receiver and transmitter, respectively, integrated with their shared local oscillator on the same GaAs substrate [24]. The four-FET switch mixer (Fig.5) used on many GaAs ICs may be very linear, but it requires large local oscillator levels to turn the switches on and off, and unlike the viable alternative of the analog multiplier, it is lossy and will degrade system noise figure.

Conventional cellular telephones typically use the double conversion architecture (Fig.8), assembled with these building blocks, often using GaAs ICs at the receiver and transmitter modules, silicon building blocks in the IF, and surrounded by an impressive collection of discrete resonator filters and antenna duplexers [25, 26]. Very small handsets [27] weighing less than 230g, and occupying a volume less than 150cc, owe more to the use of miniature discrete filters [28] and tiny IC packages [29] than to higher levels of integration in the electronics.

The new generation of digital mobile telephones, with their complex modulation formats and the greater requirements to withstand nearby blocking signals, are forcing yet greater integration of the RF and IF electronics. In a 900 MHz transmitter and receiver silicon bipolar chipset from Siemens [30], a precision quadrature upconversion mixer implements the phase-shift keyed modulation specified in the European GSM system to produce a single-sideband, suppressed carrier output. Including an output stage to drive a separate power amplifier, the IC drains 40 mA. The receiver IC includes a first mixer, with buffers to drive an IF off-chip bandpass SAW filter, and a quadrature downconversion mixer to detect the single-sideband input at baseband. Including an AGC with 70 dB range operating at the 40 to 90 MHz IF and a signal-strength indicator, the receiver IC drains 24 mA. Although the on-chip gain may be as large as 80 dB, it is distributed in different frequency bands, leading to stable operation with little on-chip crosstalk .

In an effort towards even greater miniaturization at Alcatel, the transmitter and receiver sections co-exist on one silicon bipolar chip, in this case with a zero IF architecture [31]. A separate low noise amplifier block drives directly into quadrature (I-Q) mixers with a wide enough dynamic range to withstand large blocking signals only 3 MHz away from the carrier without producing significant intermodulation. The receiver also requires large (650 pF) off-chip capacitors in an anti-alias filter, after which the quadrature downconverted signals are sent

to a baseband CMOS IC containing a high-order switched capacitor lowpass filter to remove the blocking signals, and a demodulator. An *RC* and *CR* network with off-chip trimming shifts the local oscillator phase by $\pm 45^\circ$ to produce the quadrature drive to the mixers. There are separate transmission upconversion mixers to drive a power amplifier module. The chip drains 25 mA from 5V in the receive mode, and 45mA in the transmit mode, in this respect rather similar to the Siemens chip set. Image and carrier suppression of about 40 dB is also obtained.

The frequency synthesizer in these systems is off-chip. It typically consists of a single transistor oscillator, tuned by a ceramic resonator to meet the GSM specifications of very low noise sidebands, whose frequency is varied with a series or parallel varactor diode to synthesize the receive and transmit frequencies in a variable-modulus PLL. The entire synthesizer may drain 7 mA [32].

As the local oscillator in zero IF systems is tuned to the same frequency as the received carrier, it can radiate out of the antenna and interfere with nearby receivers tuned to slightly different frequencies. However, at the typical operating power levels and with the usual RF shielding in the handset, this is apparently not such a great problem that it requires special preventive measures [33].

ICs for Spread-Spectrum Wireless Transceivers

As cellular telephones saturate the available radio frequency allocations, spread-spectrum techniques are now being deployed in cordless telephones and wireless modems [34]. These usually operate in the two lower bands allocated by the FCC for the industrial, scientific, and medical (ISM) communities for unlicensed spread-spectrum communications: 902 to 928 MHz and 2.4 to 2.83 GHz. A ubiquitous wireless environment is envisioned, where mobile users, wherever they may be, may access data and communications services through an intricate network of base stations. The greatest hardware challenge is in developing the low-power, miniature handset.

A 700 kb/s frequency-hopped spread-spectrum transceiver by Plessey operating in the 2.4 GHz band, assembled on 2"×3" PCMCIA card for insertion into notebook computers [35], is a notable recent example of miniaturization. Data is transmitted by a binary frequency-shift keying of the carrier, and the carrier frequency is slowly hopped by a variable modulus PLL

synthesizer to spread the spectrum across the entire band. All the active devices in the transceiver are on three ICs, consisting of a GaAs RF front-end, a silicon bipolar IF receiver, and a CMOS IC for the hopping frequency synthesis. Nevertheless, the transceiver requires 50 passive components, including six rather bulky filters, and it dissipates more than 1 W while transmitting 100 mW.

The single-chip GaAs IC front-end in this transceiver [36] is perhaps the most highly integrated of all the ICs discussed so far, as it includes the power amplifier and drivers for 2-GHz passive filters in the transmit and receive paths. It is otherwise a conventional double superheterodyne architecture. Interesting features are the DC series connection of the single-ended two-stage low-noise amplifier to reuse the same bias current, and that in its first version, the IC has more than 20 on-chip spiral inductors, perhaps the largest number found in any MMIC! In receive mode, the IC drains 30 mA from a 5 V supply, and with a on-chip RF switch, it can select one of two antennas to obtain spatial diversity.

ICs to Enable Future Transceivers

What will portable wireless communicators of the future look like? We may draw some conclusions from the foregoing summary of RF-IC developments to date. The crowded spectrum means that future wireless communicators will predominantly use spread-spectrum techniques, and the need for low-power dissipation will force a higher level of integration. Inspired by the modern paging receiver, which is perhaps the lowest energy wireless device in wide use, the author with his colleagues and their graduate students at UCLA is investigating the architecture and circuit design of a frequency-hopped, binary frequency-shift keyed, zero IF, all-CMOS two-chip transceiver capable of delivering up to 160 kb/s (the base ISDN rate) in the 900 MHz ISM band [37]. The transceiver ICs (Fig. 7) will freely mix analog and digital circuits, and therefore CMOS is the IC technology of choice for the entire transceiver, *including* the RF front-end. Finally, these blocks will be implemented in an unmodified standard production CMOS process.

Low-power operation requires the entire system to operate on a 3V supply, determined mainly by the analog sections and the unmodified FET threshold voltages. The power otherwise wasted in driving pad and trace parasitic capacitances is avoided with the use of on-chip inductors, whose self-resonance after the process of selective removal

of the silicon substrate (Fig.8) [38] is as high as it is on semi-insulating GaAs substrates. Thus, a 900 MHz RF amplifier with 30 dB gain draining only 3 mA has been built in 1- μ m CMOS. The problems of the mixer in a direct conversion receiver, of attaining high linearity to suppress intermodulation with interferers, as well as potential leakage of the local oscillator signal through the antenna, are both circumvented with an unusual solution: a sub-sampling downconversion mixer (Fig.9) [39]. The circuit draws 4 mA to acquire samples of a 900 MHz modulated waveform at a 50 MHz rate which it directly translates to baseband. The linearity, as measured by a +22 dBm third-order intercept, exceeds that of most continuous-time 900 MHz monolithic mixers.

Key to a frequency-hopped transceiver is a low-power, agile frequency synthesizer with adequate spectral purity. A direct-digital frequency synthesizer (DDFS) [40] produces digital words representing samples of a sine wave at an arbitrary frequency set by an input control word. Followed by a suitably linear D/A Converter, this is the ideal means to implement an agile frequency source at baseband. A CMOS implementation of a DDFS-DAC at 3 V dissipates only 40 mW, and after upconversion mixing, it spreads the signal over 902-928 MHz (Fig.10) [41]. The local oscillator consists of a four-stage MOS ring oscillator (Fig.11) locked in a PLL to a lower frequency crystal reference. The quadrature outputs at 915 MHz for the image-reject mixers are tapped off at diametrically opposite points to a phase accuracy of a couple of degrees [42]. A binary-weighted array of FETs biased near threshold, followed by a matching network, may be digitally selected to deliver power levels as high as +15 dBm to the antenna with a 30% conversion efficiency.

If successful, such a "VLSI radio" would represent a major step forward in the gradual evolution of the integrated radio as described in this paper.

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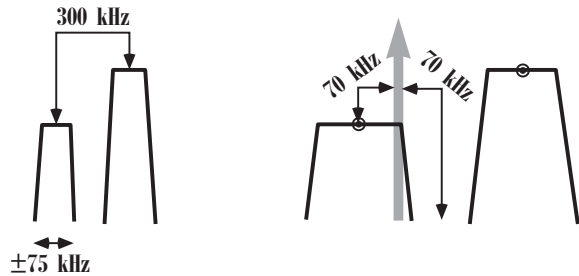


Fig.1. Channel spacing in the broadcast FM band, and the image frequency when the IF is reduced to 70 kHz [5,6].

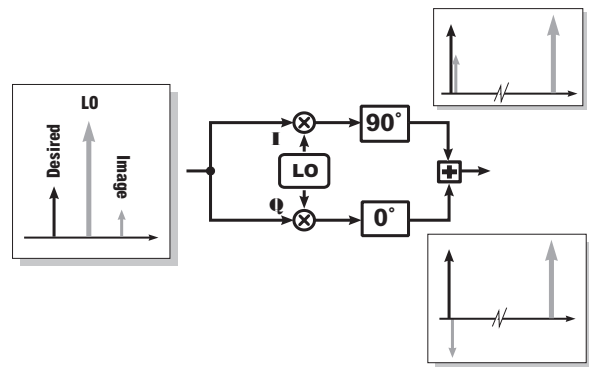


Fig.2. The image-cancelling mixer. This electronic alternative to a highly selective bandpass filter has only become practical on ICs, as the extent of image suppression depends on the matching of the two arms.

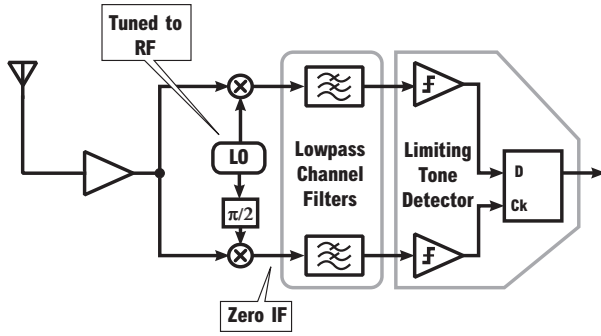


Fig.3. A simple zero IF receiver for binary FSK signals [12]. Including the lowpass channel filters, this may be readily integrated on a single IC.

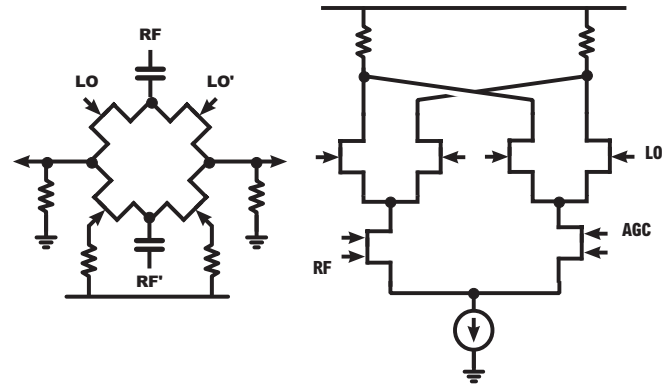


Fig.5. The double-balanced four FET switch mixer compared with a FET-tree mixer. The switch mixer affords higher linearity, but suffers from conversion loss. It is best suited for use in the transmitter upconverter.

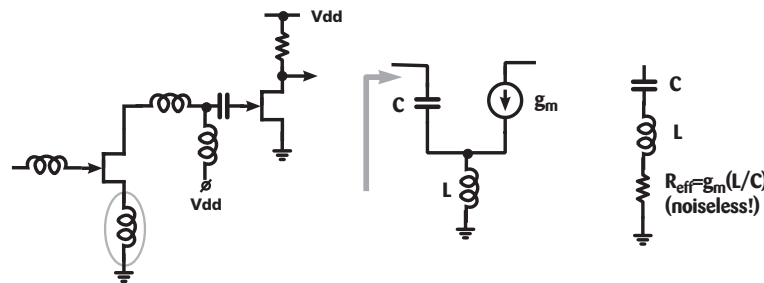


Fig.4. Typical GaAs low-noise RF amplifier uses inductors as matching elements, as tuning elements in the load, and as a noiseless degeneration element to present a resistive input impedance.

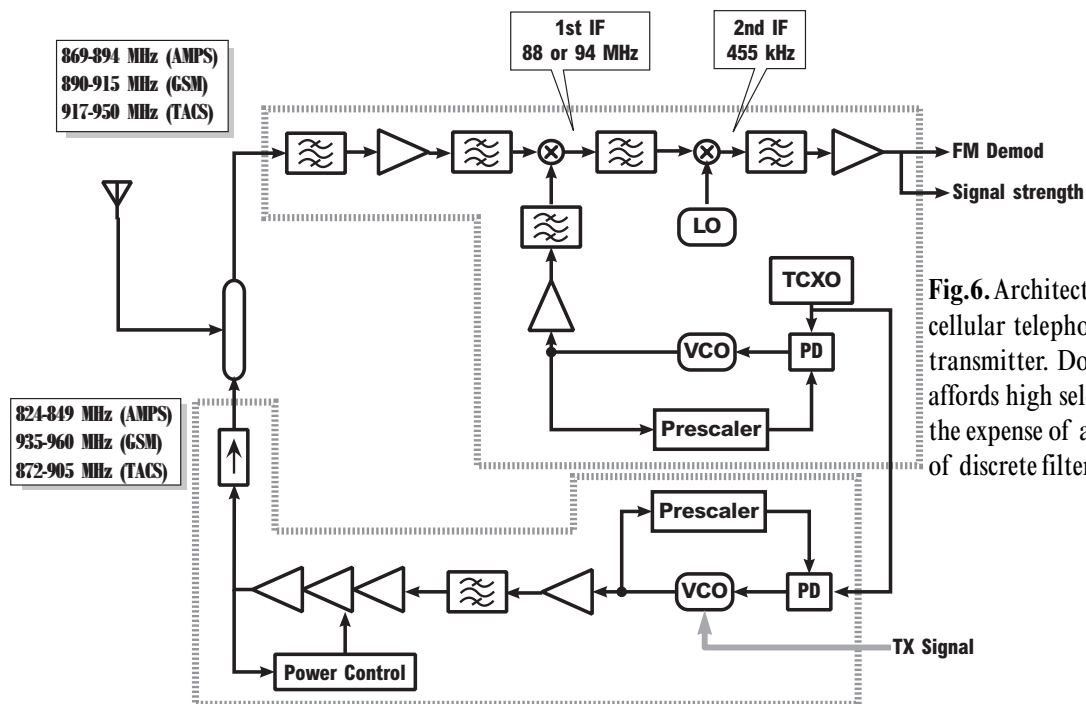


Fig.6. Architecture of a cellular telephone receiver and transmitter. Double conversion affords high selectivity, but at the expense of a large number of discrete filters.

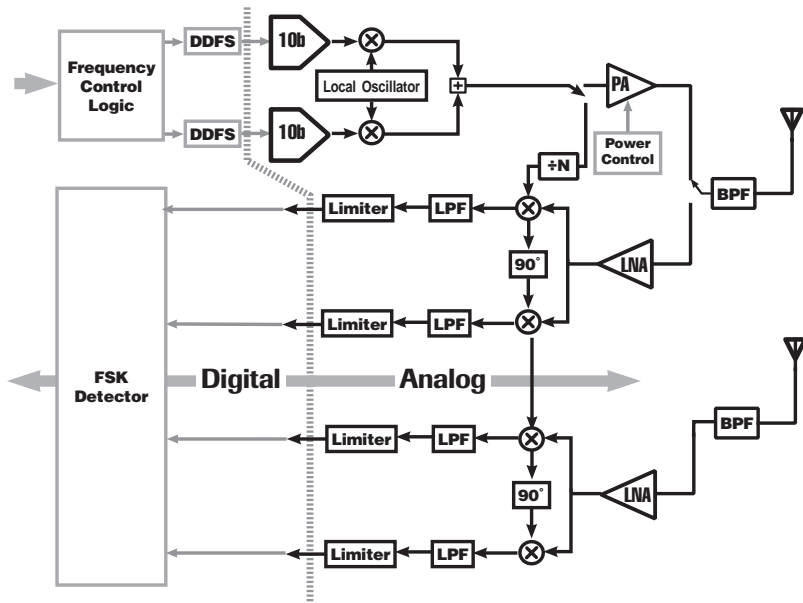


Fig.7. Architecture of the UCLA Frequency-Hopped FSK Transceiver. Two entire receive channels connected to the antennas help to combat multipath fading with spatial diversity.

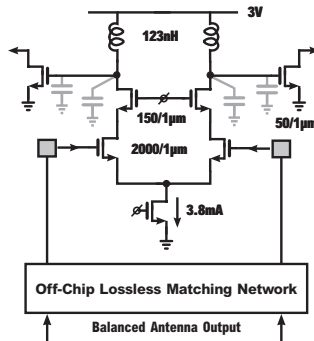
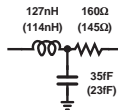
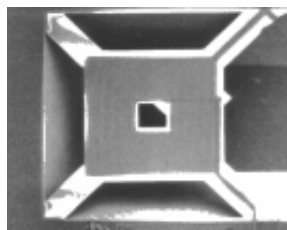


Fig.8. A 100 nH spiral inductor suspended over the silicon substrate. Self-resonance frequency is 3 GHz. A balanced CMOS RF amplifier affords 30 dB gain, 4 dB noise figure at 915 MHz.

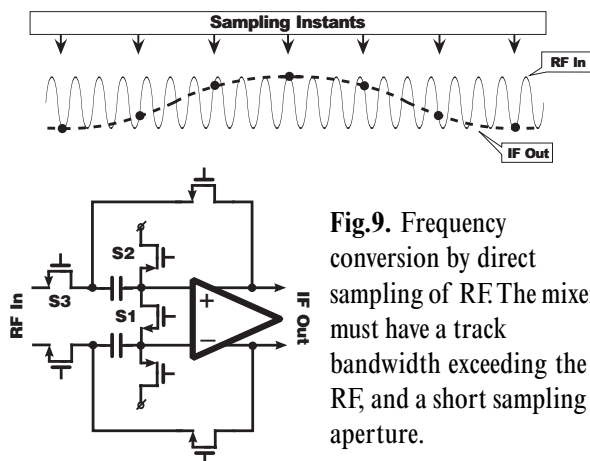


Fig.9. Frequency conversion by direct sampling of RF. The mixer must have a track bandwidth exceeding the RF, and a short sampling aperture.

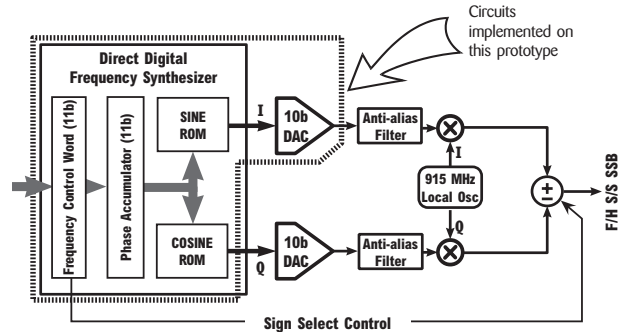


Fig.10. An agile frequency source using direct-digital frequency synthesis. Image reject mixer produces single-sideband, suppressed carrier output. Using sign selection at mixer output, upper or lower sideband may be selected, so DDFS need only span 0 to 13 MHz to cover 902-928 MHz.

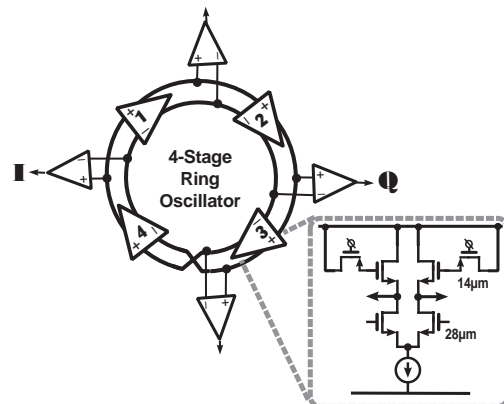


Fig.11. A 900 MHz CMOS VCO. Quadrature phases at any frequency tapped from diametrically opposite points.