Do not award half marks.
In all cases give credit for appropriate alternative answers.

Question 1 (Compulsory)

(a) Convert -32.125$_{10}$ into binary and store as a floating point normalize number using ***one's complement*** in 10-6 format (i.e. 10-bit mantissa and 6-bit exponent). [2]

-32.125$_{10}$ = - 100000.001
= - 0.100000001 x 2 ^{6}

= 1011111110 000110
mantissa exponent
[1 mark] [1 mark]

Guide: as above.

(b) The internal representation for a floating point number in two's complement mantissa and sign modulus exponent is given below. Normalize the number and show the internal representation using the same format.

11100 00001 10001 [2]
mantissa exponent

10000 00100 10011
mantissa exponent
[1 mark] [1 mark]

Guide: as above

(c) Add the following numbers given in the different systems **using decimal** and give the *final* answer in BCD (Binary Coded Decimal).

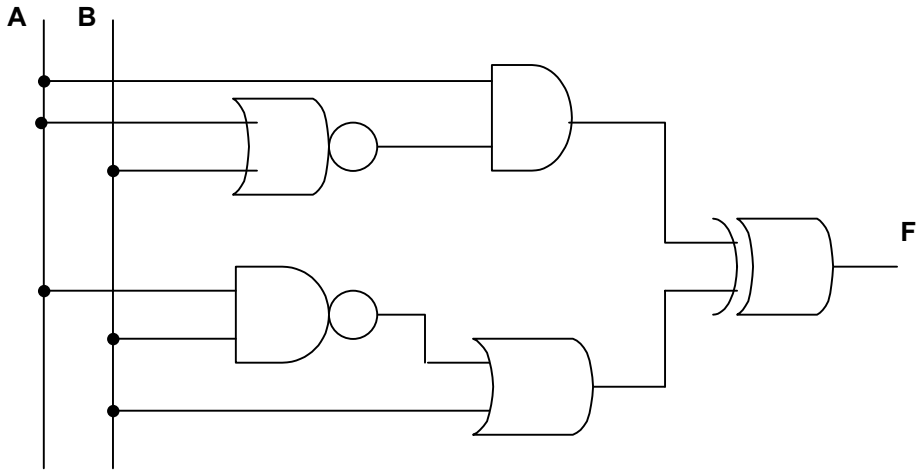
(0011$_8$ + 0011 $_{BCD}$ + 00B0$_{16}$) [3]

0011$_8$ = 8 + 1 = 9
+ 0011 $_{BCD}$ = + 3 = + 3 **[1 mark]**
+ 00B0$_{16}$) = + (11x16) = +176

(0011$_8$ + 0011 $_{BCD}$ + 00B0$_{16}$) = 188 $_{10}$ **[1 mark]**
= 0001 1000 1000 $_{BCD}$ **[1 mark]**

Guide: as above, apply consequential error for wrong conversion to answer in decimal and final answer in BCD.

(d) Get the output expression for F. Hence use Boolean algebra to simplify the expression. [3]



F = $A(A+B)'\oplus((AB)'+B)$ **[1 mark]**

= 0 $\oplus$ 1
= 00 + 11 } **[1 mark]**
= 1 **[1 mark]**

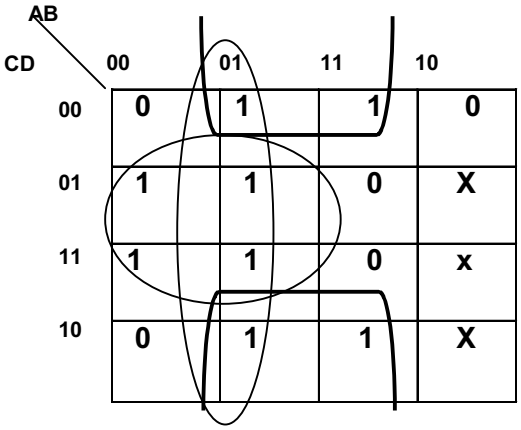
Guide: as above.

(e) Use Karnaugh map to simplify the ***four*** variable function below:

F(A,B,C,D) = π(0, 2, 8, 13, 15) + don't care (9, 10, 11)

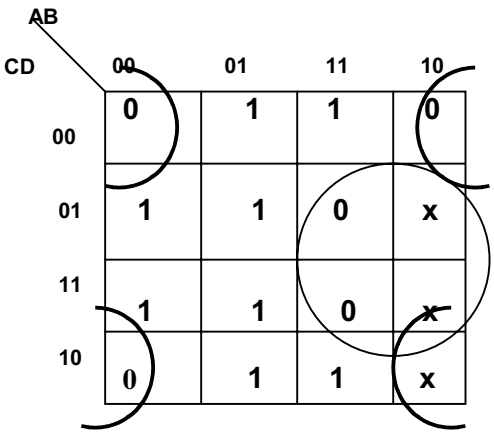
to find the SOP and POS. [5]

F(A,B,C,D) = π (0. 2, 8. 13,15) + don't care (9, 10, 11)



SOP = A'D+A'B+BD'

F(A,B,C,D) = π (0. 2, 8. 13,15) + don't care (9, 10, 11)



POS = (A'+D')(B+D)

Guide: 1 mark for the K-map and entries, 1 mark each grouping terms in the SOP and POS and 1 mark each for the SOP and POS expression.

(f) Simplify the ***six*** variable function below,

F (A, B, C, D, E, F) = Σ(m11, m15, m16, m17, m20, m21, m30, m40, m62, m63) with the use of Quine-McClusky technique. Complete the table below or otherwise get the necessary prime implicant(s) *and continue on* with the simplification. You need ***not*** redraw the whole table but just give the prime implicant(s), the plot and the final answer. [5]

F (A, B, C, D, E, F) = Σ(m11, m15, m16, m17, m20, m21, m30, m40, m62, m63)

Minterm	Binary Rep.	First Combination	Binary Rep.	Second Combination	Binary Rep.
m16	010 000	m16m17	010 00-		
m17	010 001	m16m20	010 -00		
m20	010 100	m17m21	010 -01		
m40	101 000	m20m21	010 10-		
m11	001 011	m11m15	001 -11		
m21	010 101	m30m62	-11 110		
m15	001 111	m62m63	111 11-		
m30	011 110				
m62	111 110				
m63	111 111				

F (A, B, C, D, E, F) = Σ(m11, m15, m16, m17, m20, m21, m30, m40, m62, m63)

Minterm	Binary Rep.	First Combination	Binary Rep.	Second Combination	Binary Rep.
m16	010 000	m16m17	010 00-	m16m17m20m21	010 -0-
m17	010 001	m16m20	010 -00	m16m20m17m21	010 -0-
m20	010 100	m17m21	010 -01		
m40	101 000	m20m21	010 10-		
m11	001 011	m11m15	001 -11		
m21	010 101	m30m62	-11 110		
m15	001 111	m62m63	111 11-		
m30	011 110				
m62	111 110				
m63	111 111				

[2 marks]

Prime implicants	minterms m11	m15	m16	m17	m20	m21	m30	m40	m62	m63
m40								x		
m11m15	x	x								
m30m62							x		x	
m62m63									x	x
m16m17m20m21			x	x	x	x				

[2 marks]

F (A, B, C, D, E, F)
= Σ(m11, m15, m16, m17, m20, m21, m30, m40, m62, m63)
= m40 + m11m15 + m30m62 + m62m63 + m16m17m20m21
= (101 000) + (001 -11) +(-11 110) + (111 11-)+(010 -0-)
= A B' C D' E' F' + A' B' CEF + BCDE F' +ABCDE + A' B C' E'

[1 mark]

[Total 5 marks]

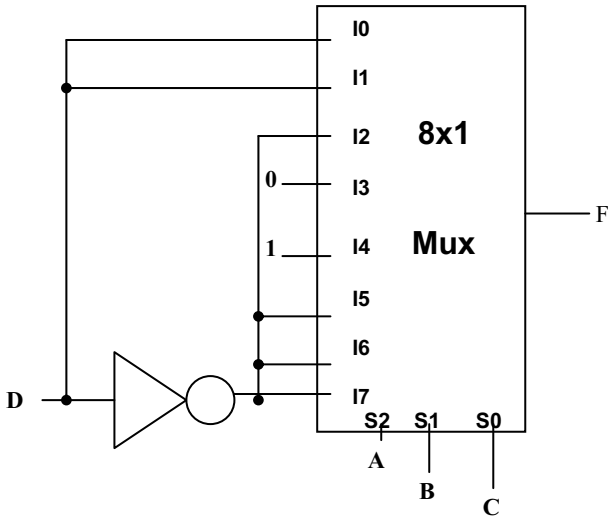
Guide: 2 marks for the table, 2 marks for the plot and 1 mark for the final expression, any of the three forms.

(g) With the use of the implementation table below or otherwise implement the function **F**(A,B,C,D) = Σ(1, 3, 4, 8, 9, 10, 12, 14). Use D as the input and A,B,C as the selector switch. Draw the diagram and neatly label it. [3]

F(A,B,C,D) = Σ (1, 3, 4, 8, 9, 10, 12, 14)

	I0	I1	I2	I3	I4	I5	I6	I7
D'	0	2	(4)	6	(8)	(10)	(12)	(14)
D	(1)	(3)	5	7	(9)	11	13	15
	D	D	D'	0	1	D'	D'	D'

Implementation Table



Guide: 1 mark for connection to inputs, 1 mark for selector and 1 mark for labeling the diagram.

(h) If a decoder has 64 *outputs*, what is the maximum number of *input*(s) that can be handled? [1]

$64 = 2^6$
hence 6 inputs

Guide: 1 mark.

(i) If an encoder has 10 *outputs*, what is the maximum number of *input*(s)? [1]

$1024 = 2^{10}$
hence 1024 inputs

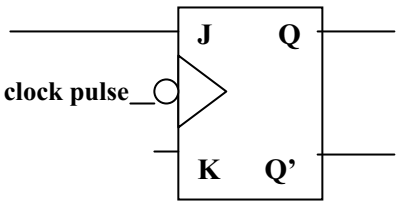
Guide: 1 mark.

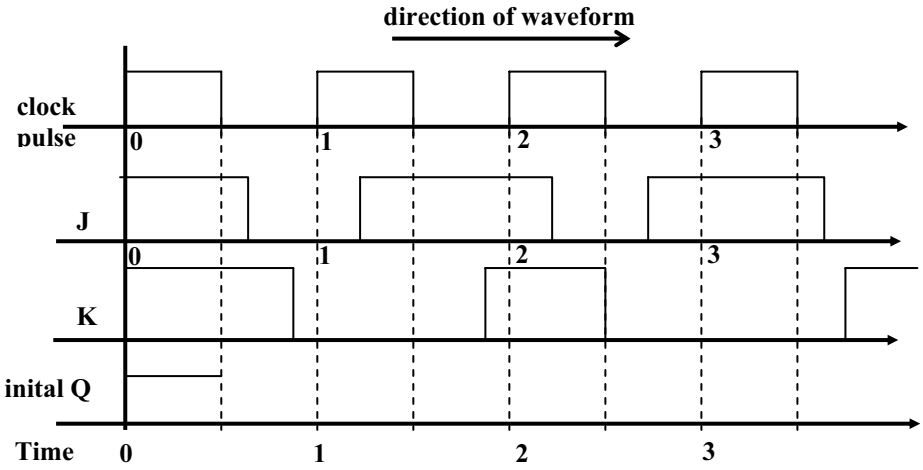
(j) How many selector(s) is /are there for a 32 x 1 demultiplexor? [1]

$32 = 2^5$
hence 5 selectors

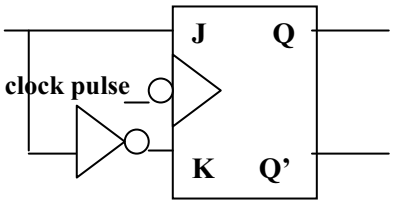
Guide: 1 mark.

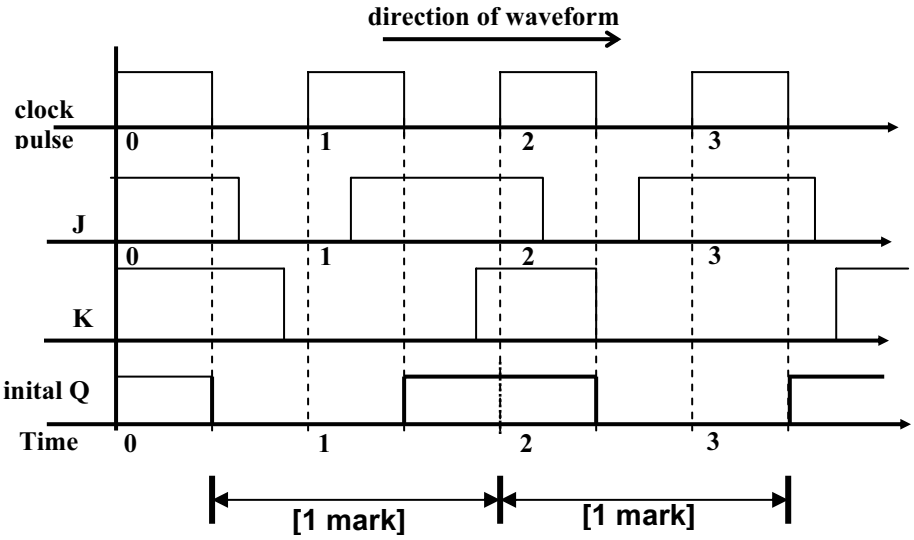
(k) Convert the JK flip-flop to a D flip-flop and sketch the waveform for the ***JK flip-flop***. The initial state of Q is given in the diagram below. [4]





Answer:





Guide: 1 mark for the NOT gate connections and 1 mark for labelling. For waveform see the above.

Question 2

(a) Give range of the ***minimum positive*** number and the ***minimum negative*** number using one's complement for both the mantissa and exponent for an 18 bit computer word in12/6 format (12 bit mantissa and 6 bit exponent). Express the answer in terms of normalized floating point format. [2]

Min. positive : 0 10000 000000 100000
Min. negative: 1 01111 111111 100000

Guide: 1 mark each.

(b) Add in Binary Coded Decimal (BCD) $128_{10} + 79_{10}$ and give the answer in decimal. [3]

$$
\begin{array}{rl}
128_{10} & \\
+\,79_{10} & = \\
 & \\
 & \\
 & \\
 & \\
 & = \\
 & 207_{10}
\end{array}
\qquad
\begin{array}{ccc}
0001 & 0010 & 1000 \\
0000 & 0111 & 1001 \\
\hline
0010 & 1010 & 0001 \\
 & 0110 & 0110 \\
\hline
0010 & 0000 & 0111
\end{array}
$$

Guide: 1 mark for two conversion to BCD, 1 mark for addition and 1 mark for final answer; working must be shown to award the final mark.

(c) **Without** converting to any other base, add directly the numbers $777_9 + 747_9$ and give the final answer in decimal. [3]

$$
\begin{array}{r}
\mathbf{777_9} \\
+\,\mathbf{747_9} \\
\hline
\mathbf{1635_9}
\end{array}
$$

1635_9 = 1X729 + 6 X 81 + 3X9 + 5
= 729 + 486 + 27 + 5
= 1247_{10}

Guide: 1 mark addition in base 9, 1 mark for working showing conversion to base 10 and 1 mark for final answer in base 10.

(d) Perform the calculation below in binary and give the answer in decimal

$(122_8 \times 4_{10} + 0022_{16}) / 8_{10}$ [3]

(122_8 = 000 001 010 010
x 4_{10} = 0000 0001 0100 1000 { ASL two places}
+ 0022_{16}) = 0000 0000 0010 0010
0000 0001 0110 1010

/ 8_{10} = 0001 0110 1. 010_2

= 32 + 8 + 4 + 1 + 0.25
= 45.25_{10}

Guide: 1 mark for Arithmetic shift left, 1 mark for arithmetic shift right and 1 mark for final answer.

(e) Add the numbers – D.0C $_{16}$ and + 0110.0101 0010 $_{BCD}$ in using two's complement for the mantissa and exponent in 10-6 format and give the final answer in decimal. [4]

(i) $-D.0C_{16}$ = - 1101. 0000 1100
= - 0.1101 0000 1100 x 2^4
= - 0.1101 0000 1 x 2^4

$0110.0101\ 0010_{BCD}$ = 6.52_{10}
= 0110.10000100_2
= 0.110 1000 01 x 2^3 **[1]**

rescale smaller number : 0. 0110 1000 0 ::1 0 x 2^4 **[1]**

complementing negative number : 1 0010 1111 1 **[1]**

add

0	**0110**	**1000 0**
1	**0010**	**1111 1**
1	**1001**	**0111 1**

[1 mark working]

= - 0. 0110 10001 000 100
= - [110 10001 x 2^{-9}] x 2^4
= - [128 + 64 + 16 +1] / 32
= - 209 / 32

= - 6.53125_{10}

[Total 4 marks]

Guide: 1 mark for two conversion, 1 mark for rescaling, 1 mark for complementing, 1 mark for working leading to the final answer. consequential error to be taken into considerations for conversion.

(f) Add the numbers - $C.0D_{16}$ and + 7.46_8 in using two's complement for the mantissa and exponent in 10-6 format and give the final answer in decimal. [4]

(i) **$-C.0D_{16}$ = - 1100. 0000 1101**
= - 0.1100 0000 1101 x 2^4

7.46_8 = 111. 100 110
= 0.111 100 110 x 2^3

rescale smaller number : 0. 011 1100 11 :: 0 x 2^4 **[1 mark]**
complementing negative number : 1. 0011 1111 0 :: 011 **[1 mark]**

add

0 0111 1001 1
1 0011 1111 0
1 1000 1000 1

[1 mark working]

= - 0. 0111 0111 0 000 100
= - [0111 0111 x 2^{-8}] x 2^4
= - [64 + 32+ 16 + 4 +2+1] / 16
= - 119 / 16

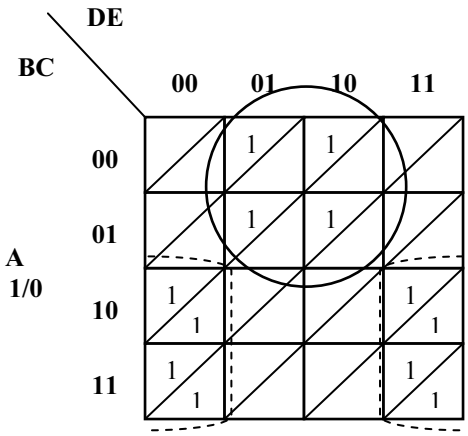
= - $\underline{7.4375_{10}}$ **[1 mark]**

[Total 4 marks]

Guide: 1 mark for rescaling, 1 mark for complementing, 1 mark for working leading to the final answer and 1 mark for final answer; consequential error to be taken into considerations for conversion.

Question 3

(a) (i) Study the 5-variable karnaugh map carefully and derive the simplified expression from the groupings in the map. [2]



F(A,B,C,D,E) = AB'E + BE'

Guide: 1 mark for each term.

(ii) simplify the expression below using another style of the five variable karnaugh map. The "X" is don't care term. [2]

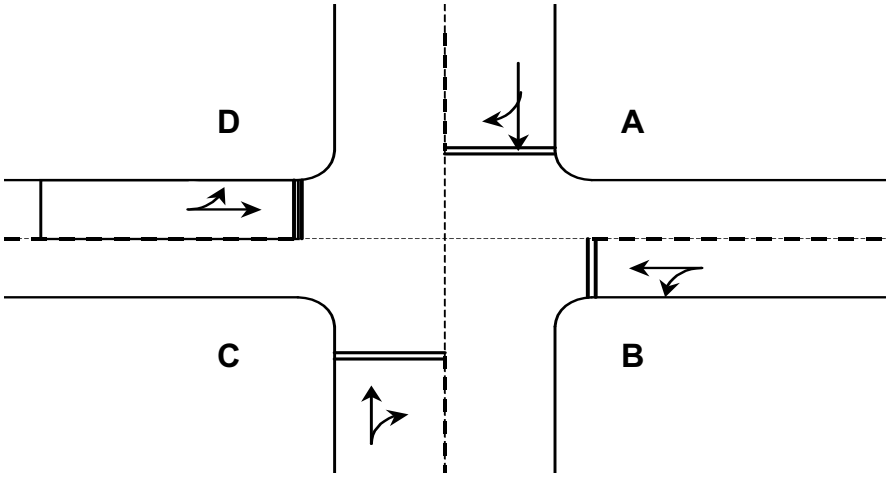
CDE / AB	000	001	011	010	110	111	101	100
00								
01				X	1			
11			1	X	X	1	1	
10			1	1	1	1	1	

F(A,B,C,D,E) = AD + BDE' + ACE

Guide: 1 mark for one correct term, 2 marks for three correct.

(b) The diagram below is that of a traffic junction controlled by four traffic light labeled A, B, C and D. The vehicles can go straight and can perform left or right turn as shown in the diagram below. When the paths intersect irrespective of whether straight or turning collision may occur and there must not be any two traffic stream entering any road at once.

Use a Boolean **'1'** to denote the traffic light is **ON** and Boolean **'0'** to denote **OFF**. Further use a Boolean **'1'** to denote **no collision** at the traffic junction and **'0' for collision**. If all the traffic lights are **ON** or **OFF** at the same time then don't bother, this is because of maintenance.



(i) Construct the truth table for the traffic junction for **no collision**. [3]

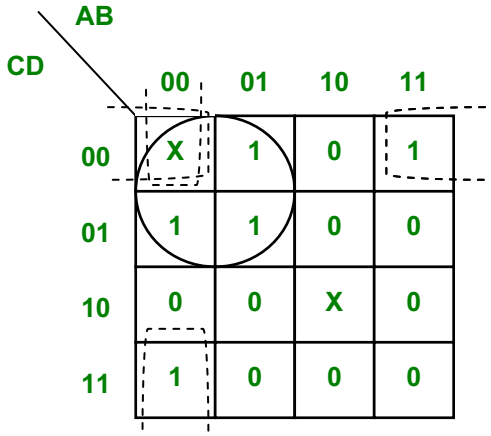
D	**01**	**01**	**01**	**01**	**01**	**01**	**01**	**01**
C	**00**	**11**	**00**	**11**	**00**	**11**	**00**	**11**
B	**00**	**00**	**11**	**11**	**00**	**00**	**11**	**11**
A	**00**	**00**	**00**	**00**	**11**	**11**	**11**	**11**
F	**X1**	**10**	**11**	**00**	**10**	**00**	**00**	**0X**

Guide: 1 mark for format of the truth table, 2 marks for the output deduct 1 mark for each error.

(ii) Get the unsimplified expression for the SOP from the truth table for **no collision**. [2]

SOP = A'B'C'D + A'B'CD'+ A'BC'D' + A'BC'D + AB'C'D'
Guide: 2 marks deduct 1 mark for each mistake.

(iii) Simplify the expression using Karnaugh map. [3]



SOP = A'B'D' + A'C' + B'C'D'

Guide: 1 mark for the K-map and entries, 1 mark grouping terms correctly and 1 mark for the final expression.

(iv) From your answer in part(iii), get the NAND implementation using Boolean algebra. You ***need not*** draw the circuit but state the laws used. [3]

SOP = A'B'D' + A'C' + B'C'D'

$$= \overline{\overline{A'B'D' + A'C' + B'C'D'}} \quad \text{(Double Complementation)}$$

$$= \overline{\overline{(A'B'D')}\ \overline{(A'C')}\ \overline{(B'C'D')}} \quad \text{(De Morgan's law)}$$

$$= \overline{\overline{(A'B'D')}\ \overline{(A'C')}\ \overline{(B'C'D')}} \quad \text{(Final Answer)}$$

Guide: 1 marks for any correct steps leading to final answer, 1 mark for any correct stated law and 1 mark for final answer.

Question 4

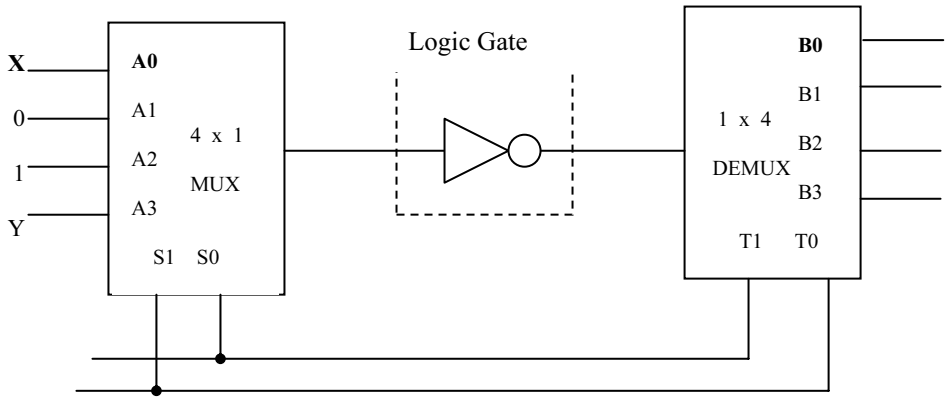
(a) (i) What is the difference between combinational and sequential circuits? [2]

For combinational circuit the output values depend only on the present value of the inputs and not on the previous values

For sequential circuit the output values depend on the present and the past inputs. In order to determine the output, the previous state must be known and hence it has memory and remembers the previous state.

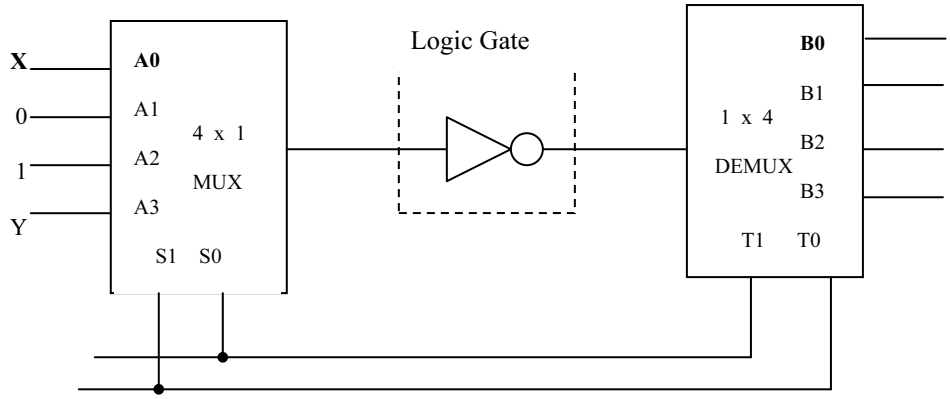
Guide: 1 mark for describing combinational circuit and 1 mark for describing sequential circuit, clarity is important for two marks.

(a) (ii) Complete the table to show the outputs B0B1B2B3 for the various values of inputs SOS1. [2]



S1	S0	B0	B1	B2	B3
0	**0**				
0	**1**				
1	**0**				
1	**1**				

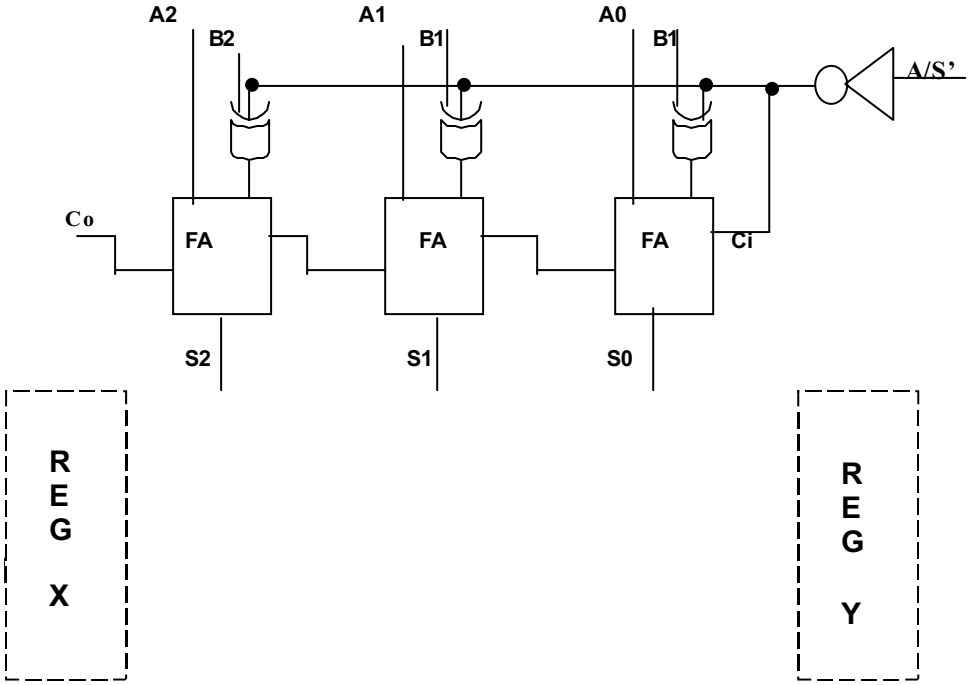
Guide: 2 marks for correct table; 1 mark for two correct rows or columns.



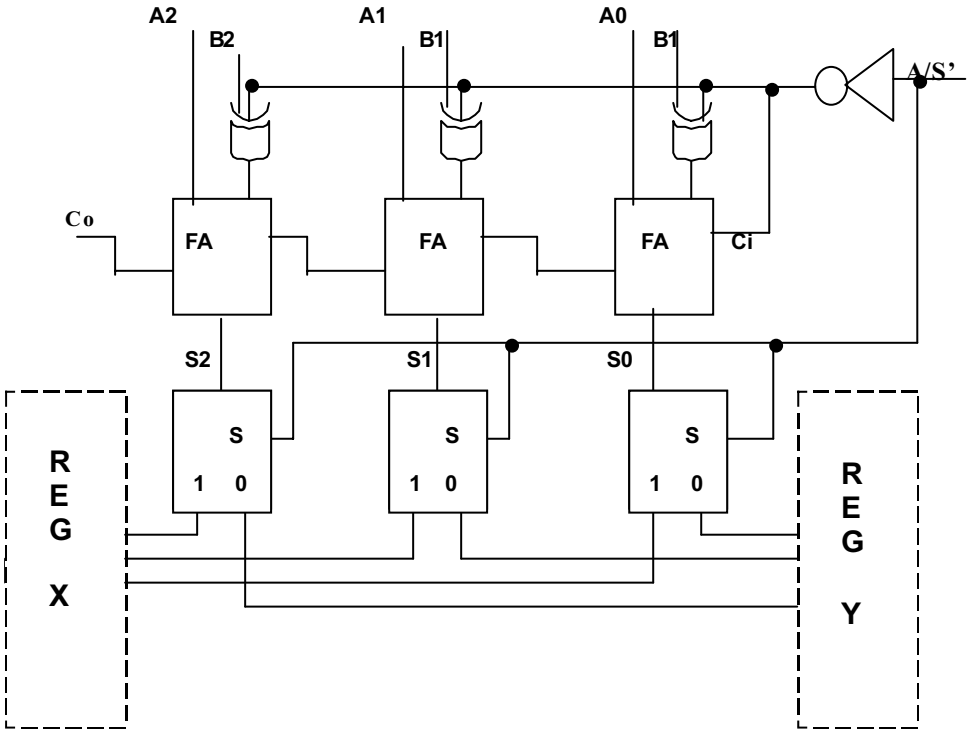
S1	S0	B0	B1	B2	B3
0	**0**	**X'**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**
1	**0**	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**	**Y'**

(b) The diagram below is a parallel adder that can add and subtract 3 binary bits. With the help of 1x2 demultiplexors, modify the design so that the results can be stored into two separate registers. The *REG X for addition* and *REG Y for subtraction*.

Draw the circuit neatly showing all the connections clearly and properly labelled. You *need not* design the registers. [4]



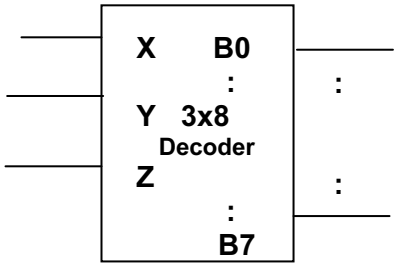
Guide: 1 mark for the A / S' switch connection to the demultiplexor switch, 1 mark for the connections to REG X, 1 mark for the connections to REG Y and 1 mark for the general connections and labeling.



(c) Construct the truth table for 3x 8 decoder and show the block diagram for it. [4]

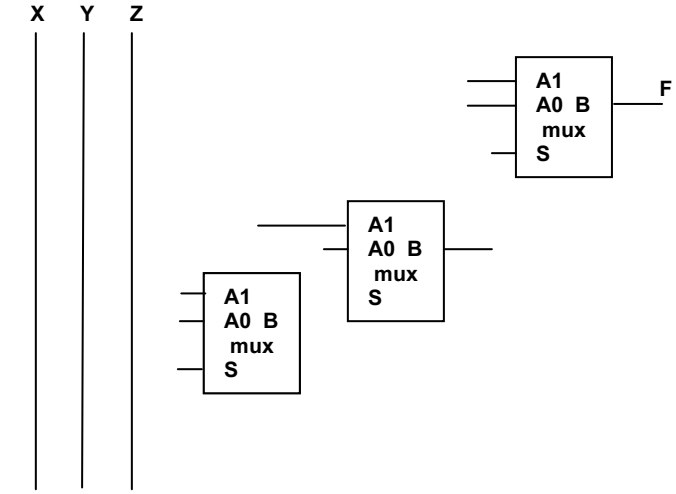
X	Y	Z	B0	B1	B2	B3	B4	B5	B6	B7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

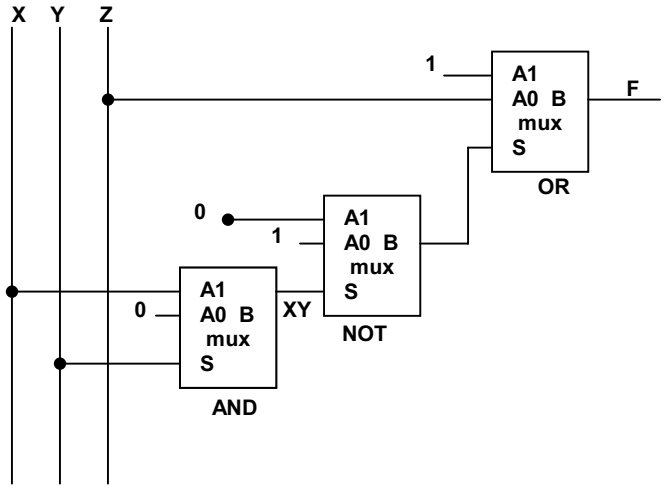
Guide: 1 mark for format of the truth table and 1 mark for the entries, if candidate show the bottom half also give the full 2 marks.



Guide: 1 mark for the block diagram and 1 mark for the labeling.

(d) The 2x1 multiplexor is a universal gate. Redraw and complete the diagram below so as to implement the Boolean function, F(X,Y,Z) = (XY)' +Z [3]





F(X,Y,Z) = (XY)' + Z

Guide: 1 mark for the AND gate connections, 1 mark for NOT gate connections 1 mark for the OR connections.

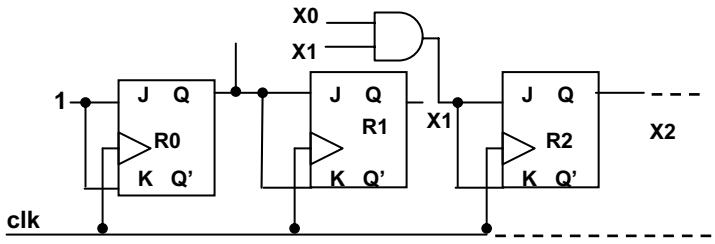
Question 5

(a) Construct the excitation (design) table of the T flip-flop. [2]

Input T	Next Qt+1
0	Qt (hold)
1	Qt' (toggle)

Guide: 1 mark for format of table and 1 mark for entries, candidates must give the excitation (design) table.

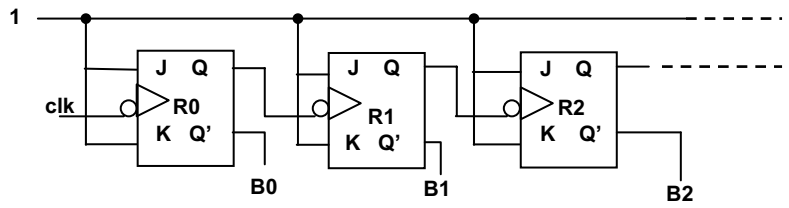
(b) A **synchronous** up-counter is to count from 0 to 63. Design the counter showing the first 3 bit using rising edge JK flip-flops and label your diagram clearly. [3]



Synchronous Up-Counter

Guide: 1 mark for connection to flip-flops, 1 mark for connection to AND gate and 1 mark for labelling diagram.

(c) An asynchronous down-counter is to count from 63 to 0. Design the counter showing the first 3 bit using the falling edge JK flip-flops and label your diagram clearly. [3]



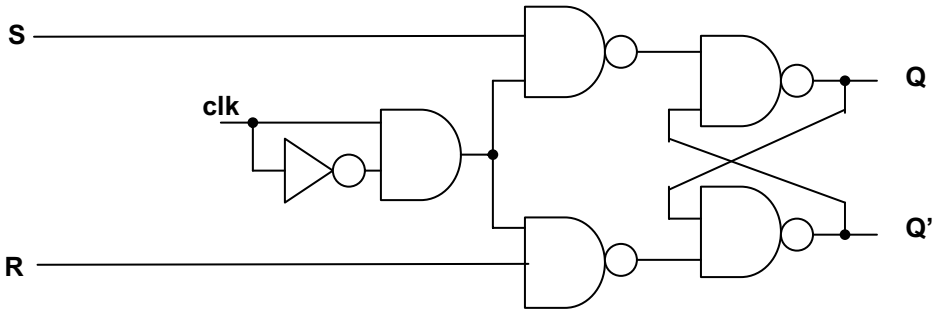
Asynchronous Down-Counter

Guide: 1 mark for the connection of '1' to flip-flop, 1 mark for connection of all flip-flops, 1 mark for labelling diagram.

(d) (i) What is the difference between level-triggered and edge-triggered flip-flops? [1]

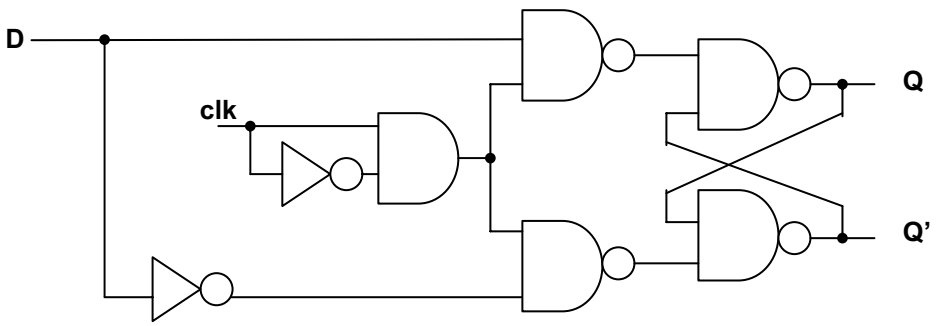
Level-triggered flip-flops respond to changes of input for half of the clock cycle; edge-triggered flip-flops read the input only on clock pulse edges.

(ii) Construct the characteristic for the edge-triggered SR flip-flop and design the positive edge trigger D flip-flop using logic gates of the SR. [4]



Previou State Q	Input S	Input R	Next State Qt+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	=
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	-

Guide: 1 mark for format of truth table and 1 mark for entries.



Guide: 1 mark for the gates and 1 mark for the connections.

(e) The ring counter can be used to step down the frequency of the clock pulse with the use of the D flip-flop. A traffic light the uses a ¼ Hz clock for amber and the time for amber light is 4 second. How many D flip-flop(s) will be required for the other lights, if the Red light is to last for 20 second and Green for 8 seconds? [2]

- **5 D flip-flop for Red**
- **2 D flip-flop for Green**

Guide 1 mark each.

- END OF PAPER -