Do not award half marks.
In all cases give credit for appropriate alternative answers.

Question 1 (Compulsory) (30 marks)

(a) What is meant by the following terms?

(i) Register addressing [2]

When a machine instruction has an operand field that contains a reference to a register [1]. The contents of the register are used as an effective address of the actual data [1].

(ii) Execute cycle [2]

The contents of an instruction register is interpreted by the appropriate decoding circuitry once the relevant data has been fetched [1]. The operation is performed and the results stored [1].

(iii) I/O direct memory access (DMA) [2]

When the I/O processor is able to transfer data directly to/from memory [1] without involvement of the CPU. [1]

(b) The width of the data bus means the number of lines in the data bus. What crucial factor is determined by the width of the data bus? [2]

The width of the data bus determines the number of bits [1] that can be transferred at a given time. [1]

(c) With the aid of a diagram, briefly explain how the effective address is determined for base addressing. [3]

There are 2 fields containing addressing information: Base field and the offset field.
Base field provides storing address of the program segment. [1]
Offset field provides displacement from a segment. [1]
To set effective address, offset in instruction is added to the base register. [1]
The diagram should include the above points to receive full credit.

(d) List any *three* network topologies and in each case provide an example application of networking where you might expect to find this topology. [6]

Award two marks each for any of the below given types.

Mesh Topology [1] Used in public and private data communication networks. [1]

Ring Topology [1] Used in LANs. [1]

Bus Topology [1] Used in LANs (Ethernet). [1]

Tree Topology/Hierarchical [1] Used in remote access corporate networks. [1]

Star Topology [1] Used in LANs with a private branch exchange (PBX), company phone systems. [1]

(e) For the following instruction mnemonics, identify the appropriate addressing modes:

(i) ADD AX, 10

(ii) ADD AX [BX + 3]

(iii) MOV AX [VAR] [3]

(i) Immediate addressing. [1]
(ii) Displacement addressing. [1]
(iii) Direct addressing. [1]

(f) Give two examples of hardware interrupts. [2]

Timer. [1]
Hard disk crash (or any other device failure). [1]
Paper jam in printer. [1]

Award credit for other acceptable answers.

(g) The operation ADD ACC, MEM uses the ALU to add the value stored in the accumulator to the value that is stored in the memory location specified in the instruction, storing the result in the accumulator. Show the steps of the execution cycle on the operation. [4]

IR decoding circuitry
MEM MAR **[1]**
MAR address bus
read control line is asserted
MEM data bus MBR **[1]**
MBR AX **[1]**
AX = Acc + MEM **[1]**

(h) Convert the below given arithmetic expression to reverse polish notation:

(A+B) * (C*(D+E)+F)) [2]

AB+DE+C*F+* **[2]**

(i) List two advantages of a Pipeline process. [2]

Improving CPU Performance (rate at which instructions are executed is much faster) [1]. Enables the processor to perform simultaneous data processing tasks. [1]

Question 2

(a) A particular cache has a capacity of *three* blocks, and begins empty. The following block request sequence is seen:

5, 4, 3, 5, 6, 5

Write down the sequence of blocks to be fetched into the cache using each of the following page replacement algorithms:

(i) Least recently used (LRU) [2]

LRU

5	5	5	5	5	5
	4	4	4	6	6
		3	3	3	3

[2]

(ii) First-in-first-out (FIFO) [2]

FIFO

5	5	5	5	6	6
	4	4	4	4	5
		3	3	3	3

[2]

(b) Cache memory is used between the CPU registers and the main memory. What is its purpose? [2]

To provide memory access speeds approaching those of the fastest available memory [1] by holding in fast memory a copy of some relevant portion of main memory. [1]

(c) Explain the need for address translation in a virtual memory system. [3]

Virtual memory systems allow programs to be run that require more memory than is available on the machine. Only parts of the program are loaded into physical memory at a time. Memory locations are accessed through the use of a page table [1].

Programs are run using virtual addresses. [1]

Virtual page number is used to match against page table entry to locate a physical page number. [1]

The physical page number is added to the offset in order to derive the actual physical address. [1]

(d) Describe the following concepts?

(i) Page swapping. [2]

When the physical memory cannot accommodate an additional page, one of the existing pages needs to be moved out of the memory [1] in order to make space. This new page is replaced into the freed page frame in memory and referenced as the current instruction. [1]

(ii) Principal of locality. [2]

States that programs access relatively small portions of the whole memory. [1]
When a block of data is fetched into the cache to satisfy a single memory reference it is likely that future references will be to other words in that block. [1]

(iii) Random access [2]

Each addressable location in memory has a unique addressable mechanism. [1] The time to access a given location is independent of the sequences of prior accesses. [1]

[6]

Question 3

(a) Compare one, two, and three-address machines by writing programs to compute.

$X = (A - B/C) * (D + E)$ [6]

1 - address:

LOAD D	**[AC] <--- [M_D]**	
ADD E	**[AC] <--- [AC] + [M_E]**	
STO R	**[M_R] <--- [AC]**	
LOA B	**[AC] <--- [M_B]**	
DIV C	**[AC] <--- [AC]/[M_C]**	
STO S	**[M_S] <--- [AC]**	
LOA A	**[AC] <--- [M_A]**	
SUB S	**[AC] <--- [M_A] – [M_S]**	**[2]**
MUL R	**[AC] <--- [AC] * [M_R]**	
STO X	**[M_X] <--- [AC]**	

2 - address:

DIV B, C	**[M_B] <--- [M_B]/[M_C]**	
SUB A, B	**[M_A] <--- [M_A] – [M_B]**	
ADD D, E	**[M_D] <--- [M_D] + [M_E]**	
MUL A, D	**[M_A] <--- [M_A] * [M_D]**	
MOV X, A	**[M_X] <--- [M_A]**	**[2]**

3 - address:

DIV B, C, R	**[M_R] <--- [M_B]/[M_C]**	
SUB A, R, S	**[M_S] <--- [M_A] – [M_R]**	
ADD D, E, T	**[M_T] <--- [M_D] + [M_E]**	
MUL S, T, X	**[M_X] <--- [M_S] * [M_T]**	**[2]**

(b) If the computer used for the above question has a 27 bit word length and the opcodes available are only those that you require, compare one, two, and three-address machines in terms of the number bits needed for the operand. [6]

1 –address

For 1- address format there are 6 distinct operations (derived from part (a)).
Therefore Size of Opcode = 3 bits (6 = 2^3 (6 is closest to 2^3) [1]
Operand needed = 27-3 = 24 bits [1]

2 - address

For 2- address format there are 5 distinct operations (derived from part (a)).
Therefore Size of Opcode = 3 bits (5 = 2^3 (5 is closest to 2^3) [1]
Operand needed = (27-3)/2 = 12 bits [1]

3 - address

For 3- address format there are 4 distinct operations (derived from part (a)).
Therefore Size of Opcode = 2 bits (4 = 2^2) [1]
Operand needed = (27-2)/3 = 8 bits [1]
(1 unused bit available)

(c) A computer system has a 4096-word memory, where each word is 64 bits wide. How many bytes does it hold? How wide must the MAR and MBR be in order to access data in this memory? [3]

Number of bytes is (4096 * (64/8)) = 32,768 [1].

Question 4

(a) Briefly define the *I/O mapped* concept. [2]

I/O mapped memory organization is where the memory and the I/O address spaces are separate. In this case the CPU must execute separate I/O instructions to activate either the read I/O or write I/O lines, which causes a word to be transferred between the addressed I/O and the CPU.

(b) The bus connects a number of different devices. Describe (with source and destination) three types of transfer that an interconnection bus structure must support. [3]

Memory to CPU: the CPU reads an instruction or a unit of data from memory. [1]
CPU to Memory: the CPU writes a unit of data to memory. [1]
I/O to CPU: the CPU reads data from an I/O device via an I/O module. [1]
I/O to or from Memory: an I/O module is allowed to exchange data directly with memory going through the CPU, using direct memory access (DMA). [1]

(c) A memory unit has the capacity of 64, 8 bit words. There are 250 different opcodes available in the instruction set. For a 3-address format, how wide is the instruction? Show all workings and illustrate your answer with the aid of a diagram. [5]

There are 250 different opcodes, so the size of the opcode = 8bits [1]
Each address (operand) is 8 bits wide. [1]
For 3-address format size of operands = 8*3 = 24 [1]
Width of the instruction word = 8+24 = 32 bits. [1]

Award [1] mark for an appropriate diagram.

(d) Typically, after an Interrupt has occurred, the Processor performs several steps to resolve the interrupting module. Describe in detail what happens to the Program, and the Processor as it initiates the Interrupt Service Routine. [5]

After the computer has been interrupted and the corresponding service program has been executed, the computer must return to exactly the same state that it was before the interrupt occurred. [1] Only if this happens will the interrupted program be able to resume exactly as if nothing has happened. [1] The state of the computer at the end of an execution of an instruction is determined from the contents of the program counter and other processor registers and the values of various status bits. [1] The collection of all status bits is sometimes called the program status word (PSW) or the status register (SR). Typically, it includes the status bits from the last ALU operation and it specifies what interrupts are allowed to occur and whether the computer is operating in a user or system mode. [1] Many computers have a resident operating system that controls and supervises all other programs. When the computer is executing programs that are part of the operating system, the computer is placed in system mode, and the computer is set in user mode when user application programs are running. [1] The mode of the computer at any given time is determined from special status bits in the PSW. [1]

Question 5

(a) List the two different types of protocols available within the transport layer of the TCP/IP suite. [2]

User Datagram Protocol (UDP) [1]
Transport Control Protocol (TCP) [1]

(b) Explain with justification why TCP/IP is considered better than OSI reference model? [3]

TCP/IP has fewer layers than OSI, and that means less performance overhead. [1]

Less complexity in implementation due to fewer layers interacting with each other. [1]

Most of the network applications are based on TCP/IP rather than OSI. [1]

Award marks for any other acceptable solutions.

(c) Explain the characteristics of static and dynamic switching techniques. [4]

Static switching

The traffic goes to all the ports in the group. [1]
Individual hubs are cheaper. [1]

Dynamic switching

The switches have to learn on which port a station is attached by studying the frames that the station transmits. [1]
Frames are transmitted only to destination stations thus saving the bandwidth of other stations. [1]
Stations are relearned every time and any change of station from one port to another is automatically reconfigured. [1]

(d) Provide any two possible solutions that overcome the bandwidth problem in Local Area Networks (LANs), explain your answer in terms of cost, performance, hardware requirements and network downtime. [6]

Possible solutions include any two of the following max. up to [2] marks :

ATM [1]
FDDI [1]
LAN Switches. [1]
Bridges and Routers. [1]

Award two marks each for any correct justification in terms of cost, performance, hardware requirement and network downtime.

- END OF PAPER -