



FEATURES

- 131,072 bytes by 8-bit organization
- Fast access time: 70ns($V_{cc}:5V\pm5\%$; $CL:35pF$)
90/120ns($V_{cc}:5V\pm10\%$; $CL:100pF$)
- Low power consumption
 - 50mA maximum active current
 - 100 μ A maximum standby current
- Programming and erasing voltage $12V \pm 5\%$
- Command register architecture
 - Byte Programming (15 μ s typical)
 - Auto chip erase 5 seconds typical (including preprogramming time)
 - Block Erase
- Optimized high density blocked architecture
 - Four 4-KB blocks
 - Seven 16-KB blocks
- Auto Erase (chip & block) and Auto Program
 - DATA polling
 - Toggle bit
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to $V_{CC}+1V$
- Advanced CMOS Flash memory technology
- Compatible with JEDEC-standard byte-wide 32-pin EPROM pinouts
- Package type:
 - 32-pin plastic DIP
 - 32-pin PLCC
 - 32-pin TSOP (Type 1)

GENERAL DESCRIPTION

The MX28F1000P is a 1-mega bit Flash memory organized as 128K bytes of 8 bits each. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F1000P is packaged in 32-pin PDIP, PLCC and TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

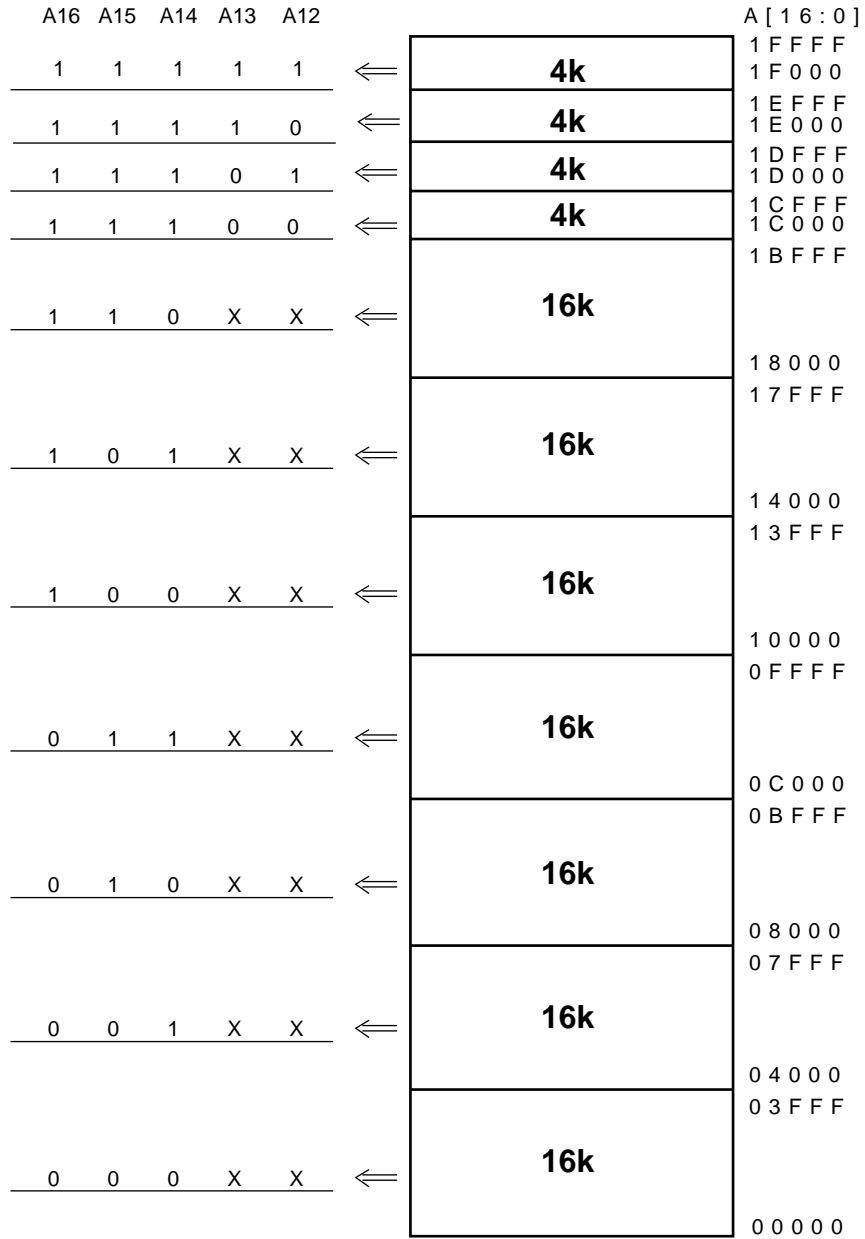
The standard MX28F1000P offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F1000P has separate chip enable (CE) and output enable (OE) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F1000P uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The

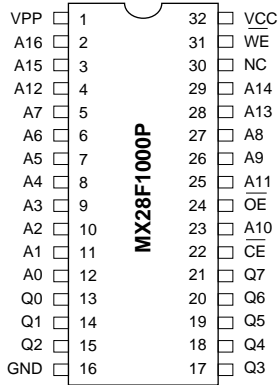
MX28F1000P uses a $12.0V \pm 5\%$ VPP supply to perform the Auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to $V_{CC} + 1V$.

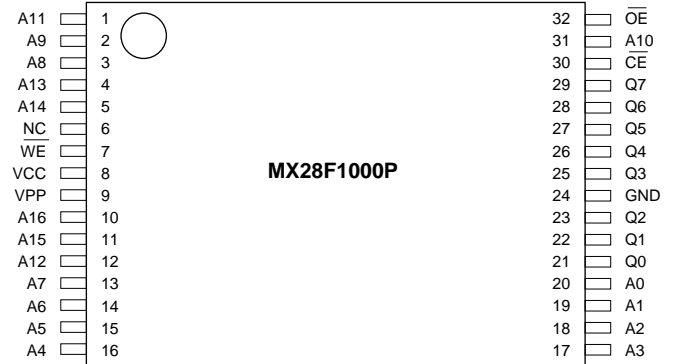
MX28F1000P Block Address and Block Structure


PIN CONFIGURATIONS

32 PDIP

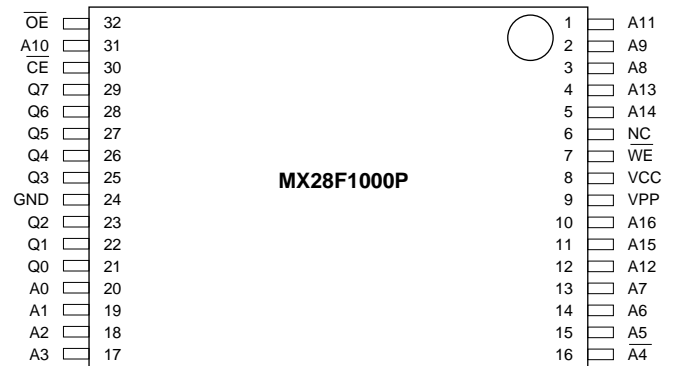
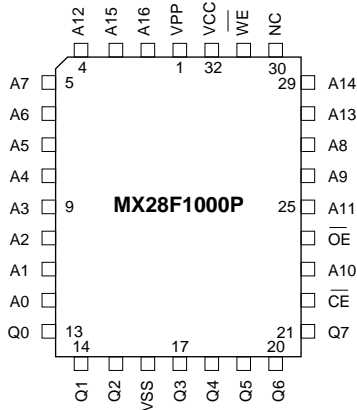


TSOP (TYPE 1)



(NORMAL TYPE)

32 PLCC

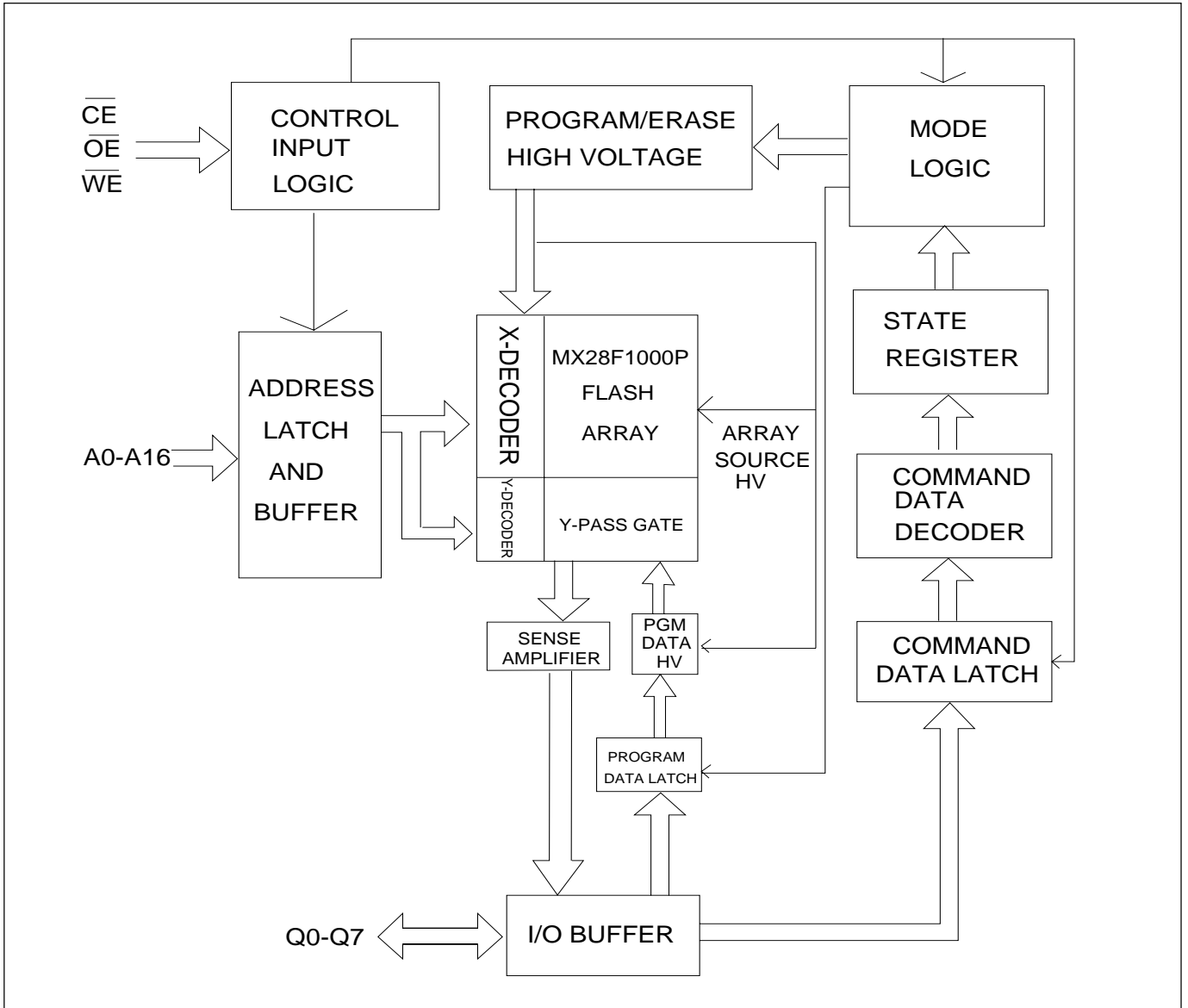


(REVERSE TYPE)

PIN DESCRIPTION:

| SYMBOL | PIN NAME |
|--------|------------------------|
| A0~A16 | Address Input |
| Q0~Q7 | Data Input/Output |
| CE | Chip Enable Input |
| OE | Output Enable Input |
| WE | Write enable Pin |
| VPP | Program Supply Voltage |
| VCC | Power Supply Pin (+5V) |
| GND | Ground Pin |

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX28F1000P is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical room temperature chip programming time of the MX28F1000P is less than 5 seconds.

AUTOMATIC CHIP ERASE

The device may be erased using the Automatic Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

AUTOMATIC BLOCK ERASE

The MX28F1000P is block(s) erasable using MXIC's Auto Block Erase algorithm. Block erase modes allow blocks of the array to be erased in one erase cycle. The Automatic Block Erase algorithm automatically programs the specified block(s) prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify, and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify, and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the MX28F1000P is designed to support either WE or CE controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of WE or CE whichever occur first. To simplify the following discussion, the WE pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the WE signal.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX28F1000P electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

TABLE 1. COMMAND DEFINITIONS

| COMMAND | BUS CYCLES | FIRST BUS CYCLE | | | SECOND BUS CYCLE | | |
|---|---------------|-----------------|---------|------|------------------|---------|------|
| | | OPERATION | ADDRESS | DATA | OPERATION | ADDRESS | DATA |
| Read Memory | 1 | Write | X | 00H | | | |
| Read Identified codes | 2 | Write | X | 90H | Read | IA | ID |
| Setup auto erase/ auto erase (chip) | 2 | Write | X | 30H | Write | X | 30H |
| Setup auto erase/ auto erase (block) | 2 | Write | X | 20H | Write | EA | D0H |
| Setup auto program/ program | 2 | Write | X | 40H | Write | PA | PD |
| Setup Erase/ Erase (chip) | 2 | Write | X | 20H | Write | X | 20H |
| Setup Erase/ Erase (block) | 2 | Write | X | 60H | Write | EA | 60H |
| Erase verify | 2 | Write | EVA | A0H | Read | X | EVD |
| Reset | 2 | Write | X | FFH | Write | X | FFH |

Note:

IA = Identifier address

EA = Block of memory location to be erased

PA = Address of memory location to be programmed

ID = Data read from location IA during device identification

PD = Data to be programmed at location PA

EVA = Address of memory location to be read during erase verify.

EVD = Data read from location EVA during erase verify.

Auto modes have the build-in enhanced features.

Please use the auto erase mode whenever it is.

COMMAND DEFINITIONS

When low voltage is applied to the VPP pin, the contents of the command register default to 00H, enabling read-only operation.

Placing high voltage on the VPP pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 1 defines these MX28F1000P register commands. Table 2 defines the bus operations of MX28F1000P.

TABLE 2. MX28F1000P BUS OPERATIONS

| OPERATION | | VPP(1) | A0 | A9 | \overline{CE} | \overline{OE} | \overline{WE} | DQ0-DQ7 |
|-------------------|-----------------------------|--------|-----|--------|-----------------|-----------------|-----------------|-------------|
| READ-ONLY | Read | VPPL | A0 | A9 | VIL | VIL | VIH | Data Out |
| | Output Disable | VPPL | X | X | VIL | VIH | VIH | Tri-State |
| | Standby | VPPL | X | X | VIH | X | X | Tri-State |
| | Read Silicon ID (Mfr)(2) | VPPL | VIL | VID(3) | VIL | VIL | VIH | Data = C2H |
| | Read Silicon ID (Device)(2) | VPPL | VIH | VID(3) | VIL | VIL | VIH | Data = 1AH |
| READ/WRITE | Read | VPPH | A0 | A9 | VIL | VIL | VIH | Data Out(4) |
| | Standby(5) | VPPH | X | X | VIH | X | X | Tri-State |
| | Write | VPPH | A0 | A9 | VIL | VIH | VIL | Data In(6) |

NOTES:

- VPPL may be grounded, a no-connect with a resistor tied to ground, or $\leq VCC + 2.0V$. VPPH is the programming voltage specified for the device. When VPP = VPPL, memory contents can be read but not written or erased.
- Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1. All other addresses are don't care.
- VID is the Silicon-ID-Read high voltage.(11.5V to 13v)
- Read operations with VPP = VPPH may access array data or Silicon ID codes.
- With VPP at high voltage, the standby current equals ICC + IPP (standby).
- Refer to Table 1 for valid Data-In during a write operation.
- X can be VIL or VIH.

READ COMMAND

While VPP is high, for erase and programming, memory contents can also be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon VPP power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the VPP power transition. Where the VPP supply is hard-wired to the MX28F1000P, the device powers up and remains enabled for reads until the command register contents are changed.

SILICON-ID-READ COMMAND

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The MX28F1000P contains a Silicon-ID-Read operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of C2H. A read cycle from address 0001H returns the device code of 1AH.

SET-UP AUTOMATIC CHIP ERASE/ERASE COMMANDS

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Automatic set-up erase command and Automatic chip erase command. Upon executing the Automatic chip erase command, the device automatically will program and verify the entire memory for an all-zero data

pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are complete when the data on DQ7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Automatic set-up erase command is a command-only operation that stages the device for automatic electrical erasure of all bytes in the array. Automatic set-up erase is performed by writing 30H to the command register.

To command automatic chip erase, the command 30H must be written again to the command register. The automatic chip erase begins on the rising edge of the WE and terminates when the data on DQ7 is "1" and the data on DQ6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

SET-UP AUTOMATIC BLOCK ERASE/ERASE COMMANDS

The automatic block erase does not require the device to be entirely pre-programmed prior to executing the Automatic set-up block erase command and Automatic block erase command. Upon executing the Automatic block erase command, the device automatically will program and verify the block(s) memory for an all-zero data pattern. The system is not required to provide any controls or timing during these operations.

When the block(s) is automatically verified to contain an all-zero pattern, a self-timed block erase and verify begin. The erase and verify operations are complete when the data on DQ7 is "1" and the data on DQ6 stops toggling for two consecutive read cycles, at which time

the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Block Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Automatic set-up block erase command is a command only operation that stages the device for automatic electrical erasure of selected blocks in the array. Automatic set-up block erase is performed by writing 20H to the command register.

To enter automatic block erase, the user must write the command D0H to the command register. Block addresses are loaded into internal register on the 2nd falling edge of WE. Each successive block load cycles, started by the falling edge of WE, must begin within 30µs from the rising edge of the preceding WE. Otherwise, the loading period ends and internal auto block erase cycle starts. When the data on DQ7 is "1" and the data on DQ6 stops toggling for two consecutive read cycles, at which time auto erase ends and the device returns to the Read mode.

SET-UP AUTOMATIC PROGRAM PROGRAM COMMANDS

Refer to page 2 for detailed block address.

The Automatic Set-up Program is a command-only operation that stages the device for automatic programming. Automatic Set-up Program is performed by writing 40H to the command register.

Once the Automatic Set-up Program operation is performed, the next WE pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the WE pulse. Data is internally latched on the rising edge of the WE pulse. The rising edge of WE also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated programming pulse and verify margin. The automatic programming operation is completed when the data read on DQ6 stops toggling for two consecutive read cycles and the data on DQ7 and DQ6 are equivalent to data written to these two bits, at which time the device returns to the Read mode (no program verify command is required).

SET-UP CHIP ERASE/ERASE COMMANDS

Set-up Chip Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the WE pulse.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the VPP pin. In the absence of this high voltage, memory contents are protected against erasure.

SET-UP BLOCK ERASE/ERASE COMMANDS

Set-up Block Erase is a command-only operation that stages the device for electrical erasure of all selected block(s) in the array. The set-up erase operation is performed by writing 60H to the command register.

To enter block-erasure, the block erase command 60H must be written again to the command register. The block erase mode allows 1 to 8 blocks of the array to be erased in one internal erase cycle. Internally, there are 8 registers (flags) addressed by A14 to A16. First block address is loaded into internal registers on the 2-nd falling of WE. Each successive block load cycles, started by the falling edge of WE, must begin within 30µs from the rising edge of the preceding WE. Otherwise, the loading period ends and internal block erase cycle starts. When the data on DQ7 is "1" at which time auto erase ends and the device returns to the Read mode.

ERASE-VERIFY COMMAND

After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the

falling edge of the WE pulse.

The MX28F1000P applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/ Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. The High Reliability Erase algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the MX28F1000P.

RESET COMMAND

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. Should program-fail or erase-fail happen, two consecutive writes of FFH will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

WRITE OPERATON STATUS

TOGGLE BIT-DQ6

The MX28F1000P features a "Toggle Bit" as a method to indicate to the host sytem that the Auto Program/ Erase algorithms are either in progress or completed.

While the Automatic Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Automatic Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the second WE pulse of the two write pulse sequences.

DATA POLLING-DQ7

The MX28F1000P also features Data Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to DQ7. Upon completion of the Automatic Program algorithm an attempt to read the device will produce the true data last written to DQ7. The Data Polling feature is valid after the rising edge of the second WE pulse of the two write pulse sequences.

While the Automatic Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The Data Polling feature is valid after the rising edge of the second WE pulse of two write pulse sequences.

The Data Polling feature is active during Automatic Program/Erased algorithms.

POWER-UP SEQUENCE

The MX28F1000P powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. Power up sequence is not required.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND, and between VPP and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on FLASH memory arrays, a 4.7 μ F bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

ABSOLUTE MAXIMUM RATINGS

| RATING | VALUE |
|-------------------------------|----------------|
| Ambient Operating Temperature | 0°C to 70°C |
| Storage Temperature | -65°C to 125°C |
| Applied Input Voltage | -0.5V to 7.0V |
| Applied Output Voltage | -0.5V to 7.0V |
| VCC to Ground Potential | -0.5V to 7.0V |
| A9 & VPP | -0.5V to 13.5V |

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25°C, f = 1.0 MHz

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|--------|--------------------|------|-----|------|------|------------|
| CIN | Input Capacitance | | | 14 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 16 | pF | VOUT = 0V |

READ OPERATION
DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|--------|------------------------|--------------|-----|-----------|------|---------------------------------|
| ILI | Input Leakage Current | | | 10 | μA | VIN = GND to VCC |
| ILO | Output Leakage Current | | | 10 | μA | VOUT = GND to VCC |
| IPP1 | VPP Current | | 1 | 100 | μA | VPP = 5.5V |
| ISB1 | Standby VCC current | | | 1 | mA | $\overline{CE} = V_{IH}$ |
| ISB2 | | | 1 | 100 | μA | $\overline{CE} = V_{CC} + 0.3V$ |
| ICC1 | Operating VCC current | | | 30 | mA | IOUT = 0mA, f=1MHz |
| ICC2 | | | | 50 | mA | IOUT = 0mA, f=11MHz |
| VIL | Input Low Voltage | -0.3(NOTE 1) | | 0.8 | V | |
| VIH | Input High Voltage | 2.4 | | VCC + 0.3 | V | |
| VOL | Output Low Voltage | | | 0.45 | V | IOL = 2.1mA |
| VOH | Output High Voltage | 2.4 | | | V | IOH = -400μA |

NOTES:

- VIL min. = -1.0V for pulse width ≤ 50 ns.
VIL min. = -2.0V for pulse width ≤ 20 ns.
- VIH max. = VCC + 1.5V for pulse width ≤ 20 ns
If VIH is over the specified maximum value, read operation cannot be guaranteed.
- Test condition:
TA = 0°C to 70°C, Vcc = 5V±10%, Vpp = GND to Vcc, CL = 100pF(for MX28F1000P-90/12)
TA = 0°C to 70°C, Vcc = 5V±10%, Vpp = GND to Vcc, CL = 35pF(for MX28F1000P-70)

AC CHARACTERISTICS

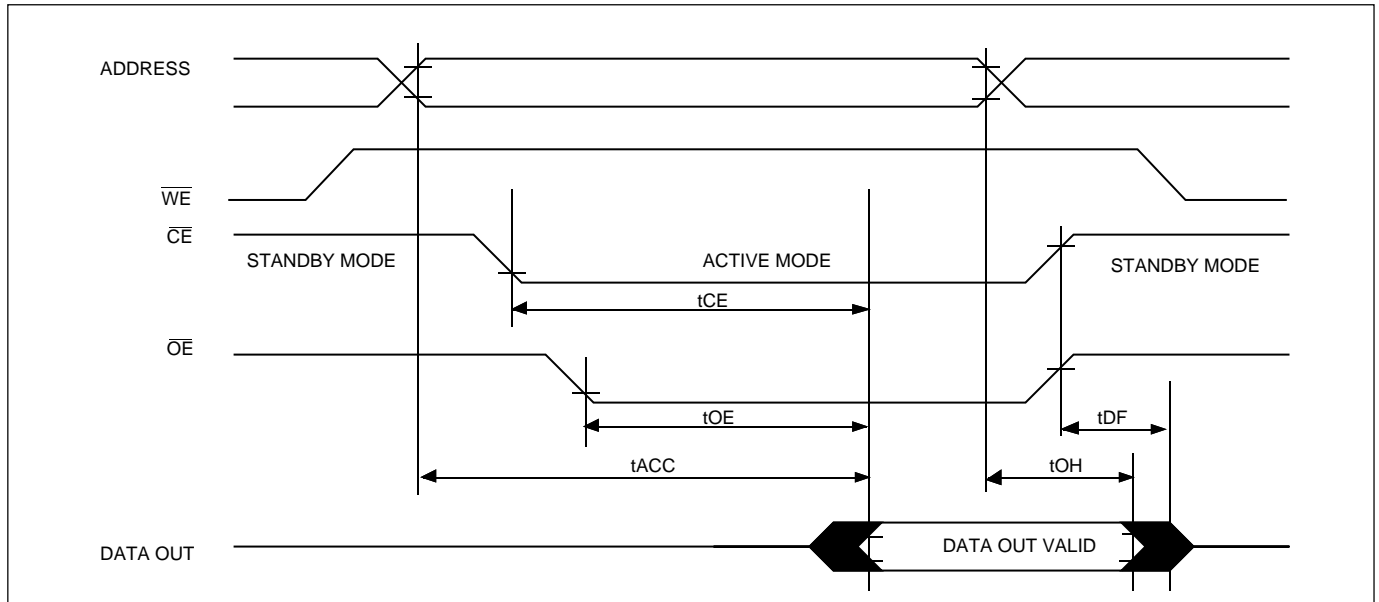
| SYMBOL | PARAMETER | 28F1000P-70 | | 28F1000P-90 | | 28F1000P-12 | | UNIT | CONDITIONS |
|--------|--|-------------|------|-------------|------|-------------|------|------|--|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| tACC | Address to Output Delay | | 70 | | 90 | | 120 | ns | $\overline{CE}=\overline{OE}=\text{VIL}$ |
| tCE | \overline{CE} to Output Delay | | 70 | | 90 | | 120 | ns | $\overline{OE}=\text{VIL}$ |
| tOE | \overline{OE} to Output Delay | | 30 | | 35 | | 50 | ns | $\overline{CE}=\text{VIL}$ |
| tDF | \overline{OE} High to Output Float (Note1) | 0 | 15 | 0 | 20 | 0 | 30 | ns | $\overline{CE}=\text{VIL}$ |
| tOH | Address to Output hold | 0 | 0 | 0 | 0 | 0 | 0 | ns | $\overline{CE}=\overline{OE}=\text{VIL}$ |

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: $\leq 10\text{ns}$
- Reference levels for measuring timing: 0.8V, 2.0V
- 28F1000P-70: $V_{CC} = 5V \pm 5\%$, CL: 1TTL gate + 35pF(including scope and jig)
- 28F1000P-90: $V_{CC} = 5V \pm 5\%$, CL: 1TTL gate + 35pF(including scope and jig)
- $V_{pp} = \text{GND to } V_{CC}$

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS


**COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION
DC CHARACTERISTICS**

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|-----------------------|------------------------|---------------|-----|----------------------|------|------------------------------|
| ILI | Input Leakage Current | | | 10 | μA | VIN=GND to VCC |
| ILO | Output Leakage Current | | | 10 | μA | VOUT=GND to VCC |
| ISB1 | Standby VCC current | | | 1 | mA | $\overline{CE}=VIH$ |
| ISB2 | | | 1 | 100 | μA | $\overline{CE}=VCC \pm 0.3V$ |
| ICC1 (Read) | Operating VCC Current | | | 30 | mA | IOUT=0mA, f=1MHz |
| ICC2 | | | | 50 | mA | IOUT=0mA, F=11MHz |
| ICC3 (Program) | | | | 50 | mA | In Programming |
| ICC4 (Erase) | | | | 50 | mA | In Erase |
| ICC5 (Program Verify) | | | | 50 | mA | In Program Verify |
| ICC6 (Erase Verify) | | | | 50 | mA | In Erase Verify |
| IPP1 (Read) | | VPP Current | | | 100 | μA |
| IPP2 (Program) | | | | 50 | mA | In Programming |
| IPP3 (Erase) | | | | 50 | mA | In Erase |
| IPP4 (Program Verify) | | | | 50 | mA | In Program Verify |
| IPP5 (Erase Verify) | | | | 50 | mA | In Erase Verify |
| VIL | Input Voltage | -0.3 (Note 5) | | 0.8 | V | |
| VIH | | 2.4 | | VCC+0.3V (Note 6) | V | |
| VOL | Output Voltage | | | 0.45 | V | IOL=2.1mA |
| VOH | | 2.4 | | | V | IOH=-400μA |

NOTES:

- VCC must be applied before VPP and removed after VPP.
- VPP must not exceed 14V including overshoot.
- An influence may be had upon device reliability if the device is installed or removed while VPP=12V.
- Do not alter VPP either VIL to 12V or 12V to VIL when $\overline{CE}=VIL$.
- VIL min. = -0.6V for pulse width $\leq 20ns$.
- If VIH is over the specified maximum value, programming operation cannot be guaranteed.
- All currents are in RMS unless otherwise noted. (Sampled, not 100% tested.)
- For 28F1000P-70, Vcc = 5V $\pm 5\%$, CL = 35pF; for 28F1000P-90/12, Vcc = 5V $\pm 10\%$, CL = 100pF.

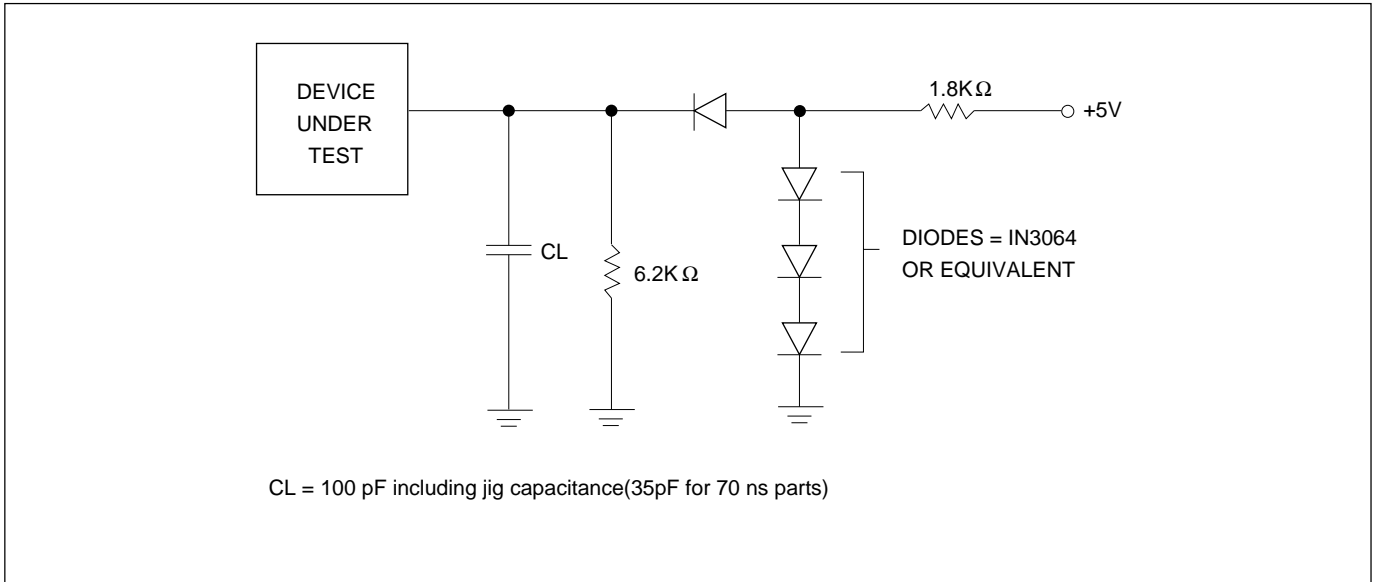
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = 12V ± 5%

| SYMBOL | PARAMETER | 28F1000-70 | | 28F1000P-90 | | 28F1000P-12 | | UNIT | CONTIONS |
|--------|--|------------|------|-------------|------|-------------|------|------|----------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| tVPS | VPP setup time | 100 | | 100 | | 100 | | ns | |
| tOES | \overline{OE} setup time | 100 | | 100 | | 100 | | ns | |
| tCWC | Command programming cycle | 70 | | 90 | | 120 | | ns | |
| tCEP | \overline{WE} programming pulse width | 40 | | 45 | | 50 | | ns | |
| tCEPH1 | \overline{WE} programming pluse width High | 20 | | 20 | | 20 | | ns | |
| tCEPH2 | \overline{WE} programming pluse width High | 100 | | 100 | | 100 | | ns | |
| tAS | Address setup time | 0 | | 0 | | 0 | | ns | |
| tAH | Address hold time | 40 | | 45 | | 50 | | ns | |
| tAH1 | Address hold time for \overline{DATA} POLLING | 0 | | 0 | | 0 | | ns | |
| tDS | Data setup time | 40 | | 45 | | 50 | | ns | |
| tDH | Data hold time | 10 | | 10 | | 10 | | ns | |
| tCESP | \overline{CE} setup time before \overline{DATA} polling/toggle bit | 100 | | 100 | | 100 | | ns | |
| tCES | \overline{CE} setup time | 0 | | 0 | | 0 | | ns | |
| tCESC | \overline{CE} setup time before command write | 100 | | 100 | | 100 | | ns | |
| tCESV | \overline{CE} setup time before verify | 6 | | 6 | | 6 | | μs | |
| tVPH | VPP hold time | 100 | | 100 | | 100 | | ns | |
| tDF | Output disable time (Note 3) | | 15 | | 20 | | 30 | ns | |
| tDPA | \overline{DATA} polling/toggle bit access time | | 70 | | 90 | | 120 | ns | |
| tAETC | Total erase time in auto chip erase | 5(TYP.) | | 5(TYP.) | | 5(TYP.) | | s | |
| tAETB | Total erase time in auto block erase | 5TYP.) | | 5(TYP.) | | 5(TYP.) | | s | |
| tAVT | Total programming time in auto verify | 15 | 300 | 15 | 300 | 15 | 300 | μs | |
| tBALC | Block address load cycle | 0.3 | 30 | 0.3 | 30 | 0.3 | 30 | μs | |
| tBAL | Block address load time | 200 | | 200 | | 200 | | μs | |
| tCH | \overline{CE} Hold Time | 0 | | 0 | | 0 | | ns | |
| tCS | \overline{CE} setup to \overline{WE} going low | 0 | | 0 | | 0 | | ns | |

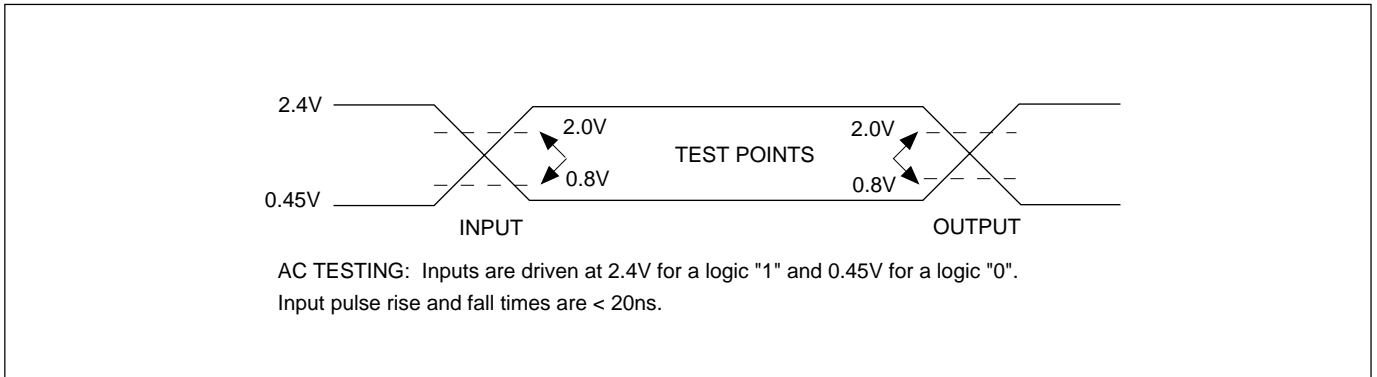
NOTES:

1. \overline{CE} and \overline{OE} must be fixed high during VPP transition from 5V to 12V or from 12V to 5V.
2. Refer to read operation when VPP=VCC about read operation while VPP 12V.
3. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

SWITCHING TEST CIRCUITS



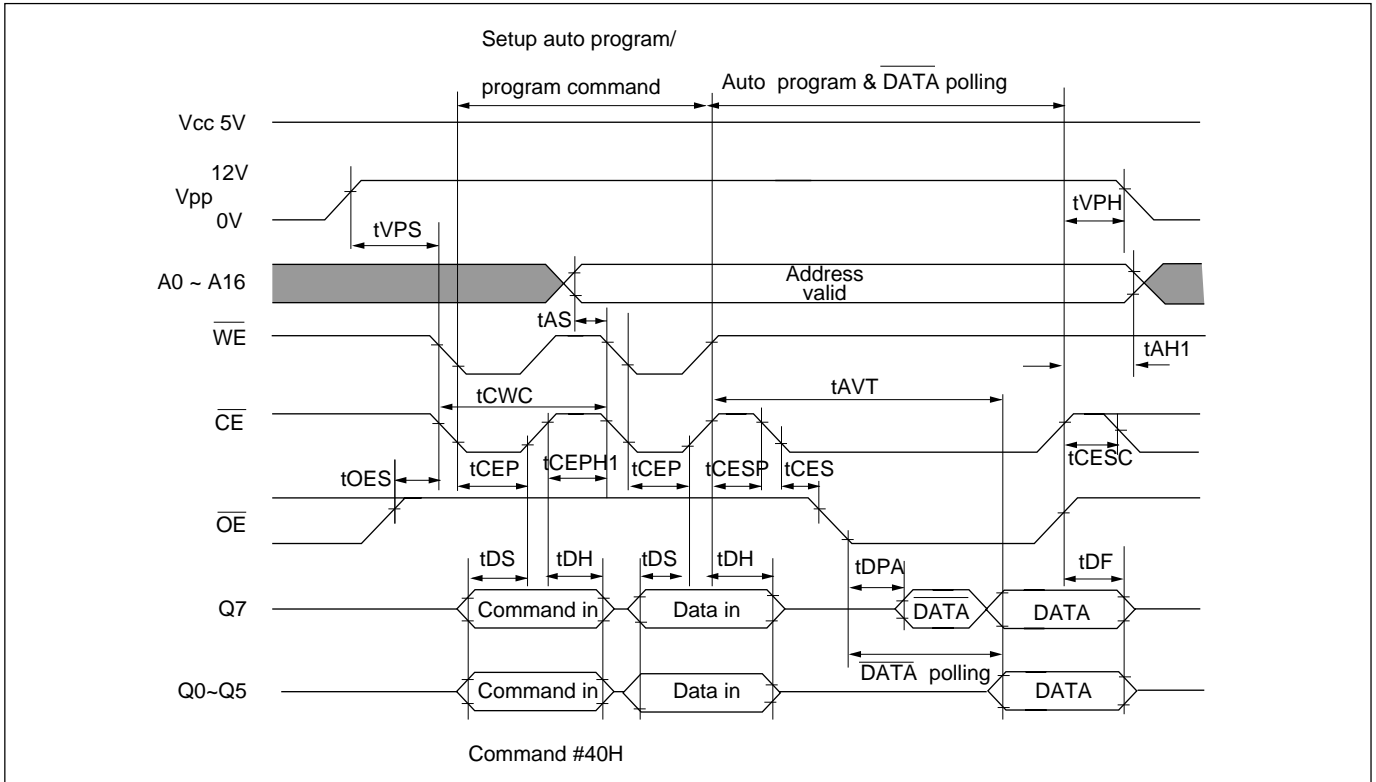
SWITCHING TEST WAVEFORMS

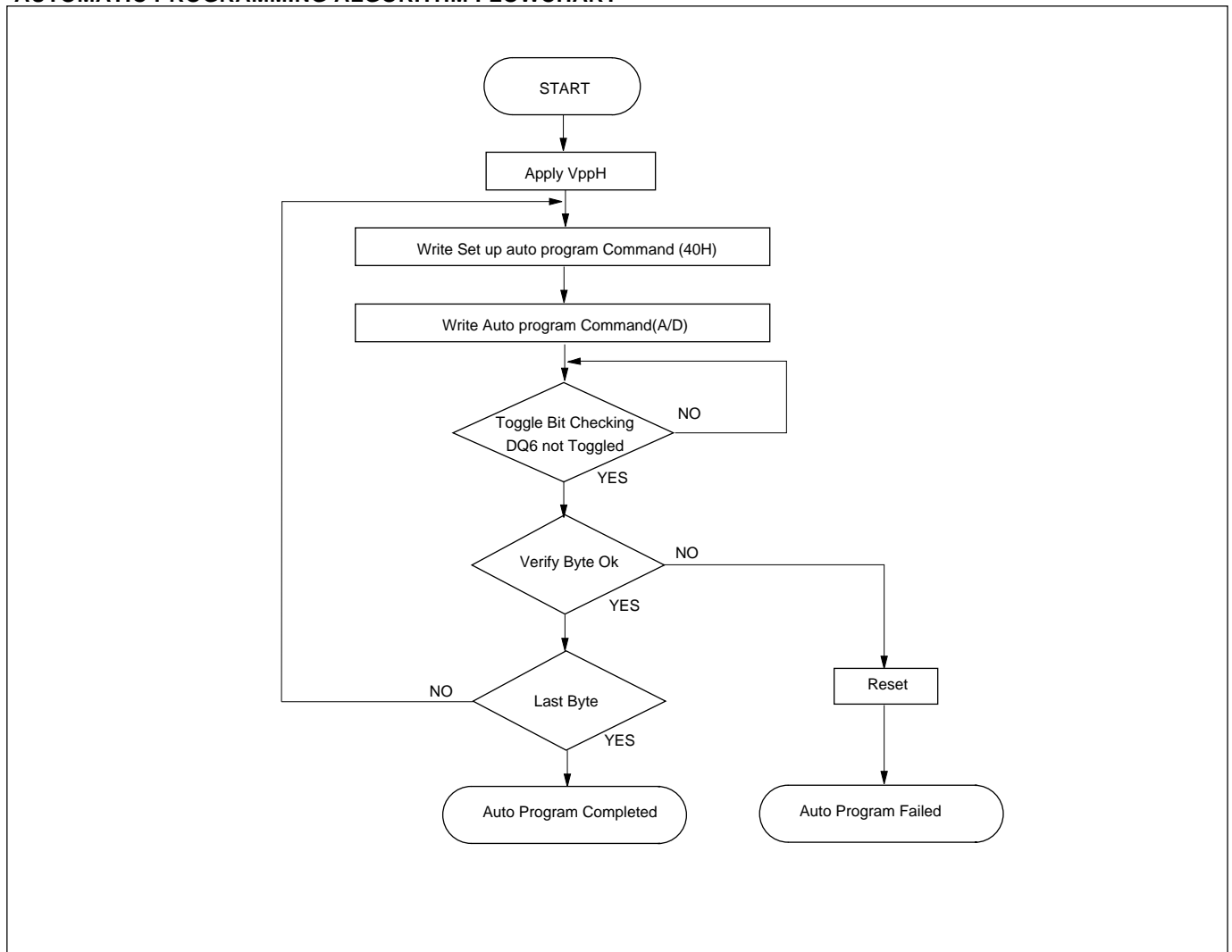


AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by DATA polling and toggle bit

checking after automatic verify starts. Device outputs DATA during programming and DATA after programming on Q7. Q0 to Q5 (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform) are in high impedance.

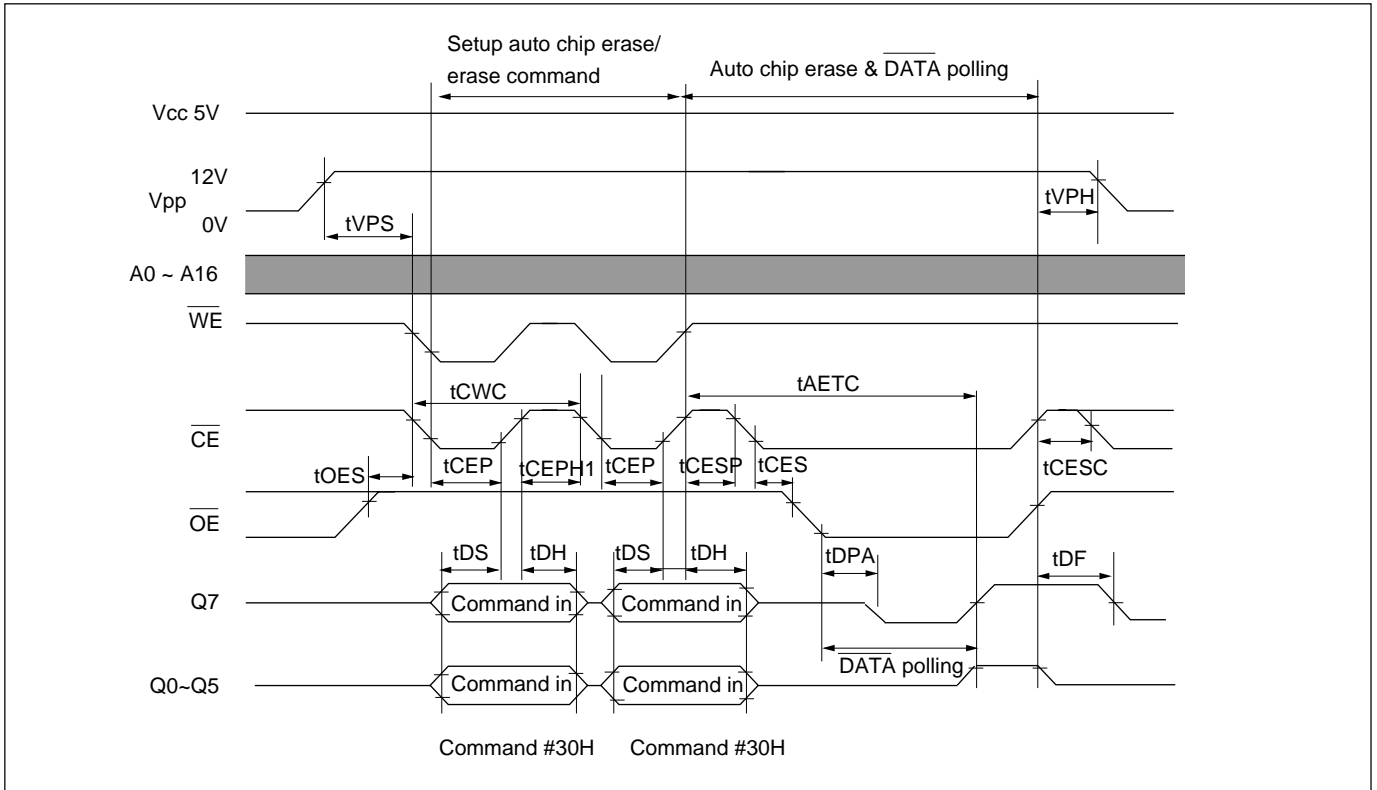


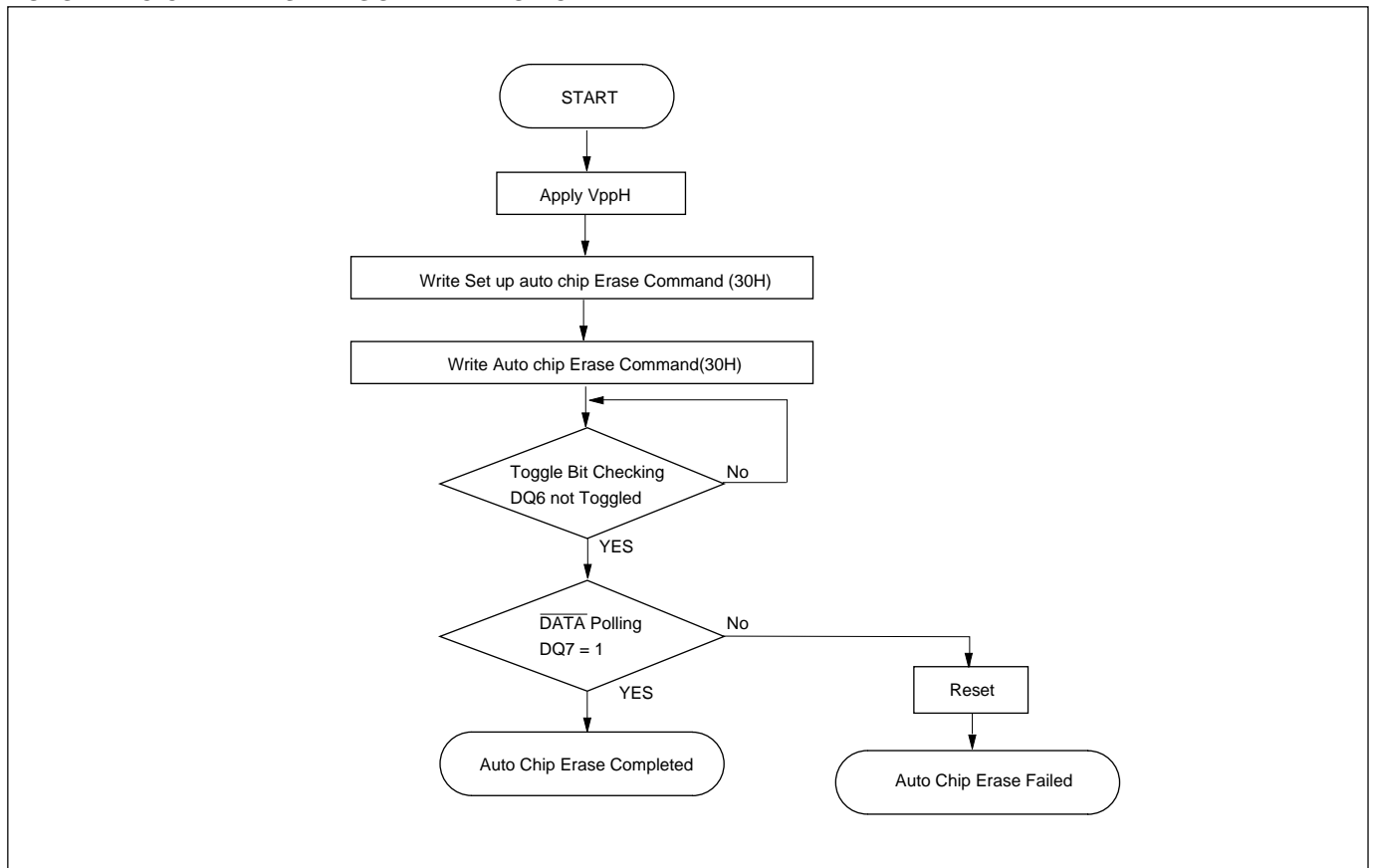
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verify is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic

erase starts. Device outputs 0 during erasure and 1 after erasure on Q7. Q0 to Q5 (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform) are in high impedance.

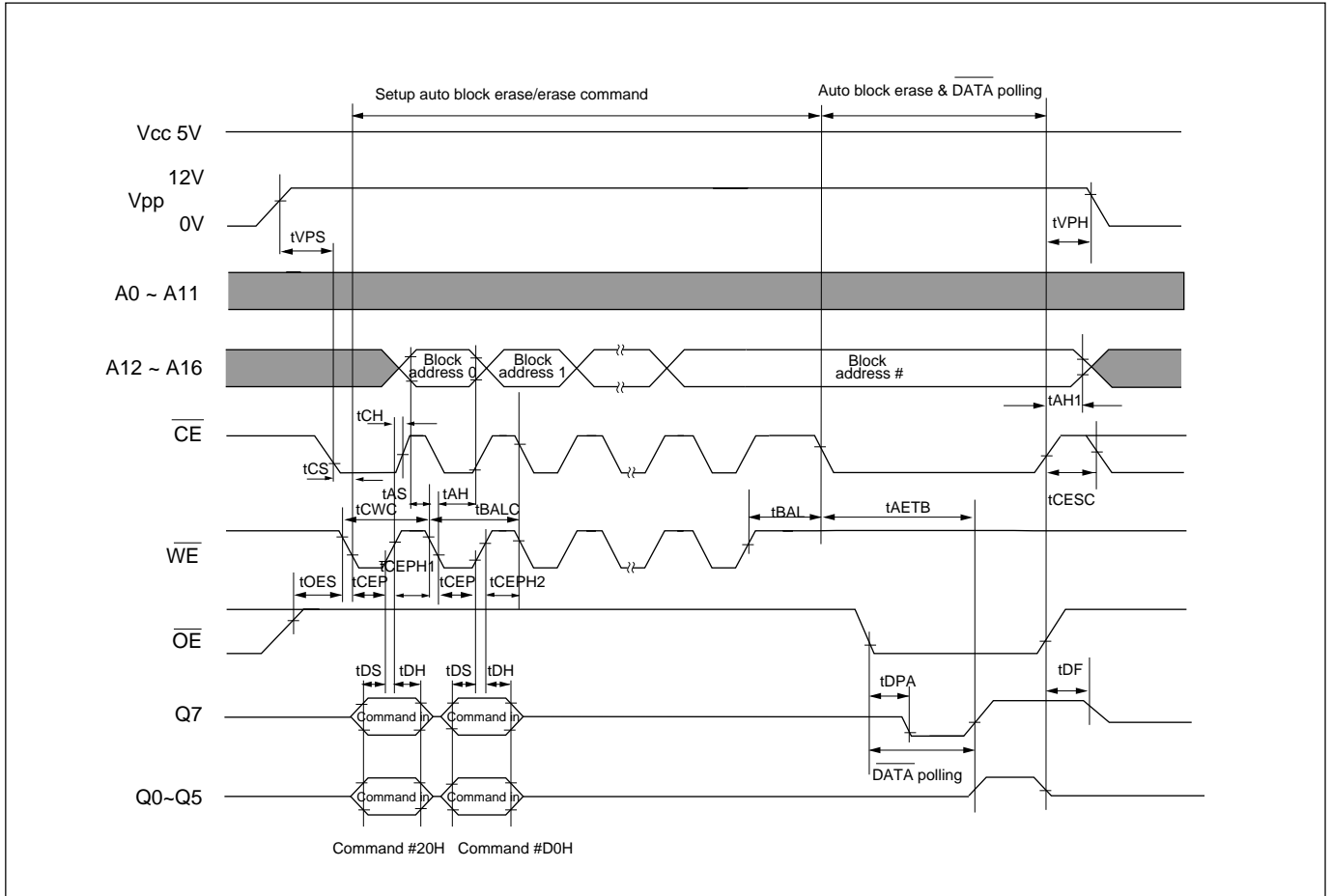


AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

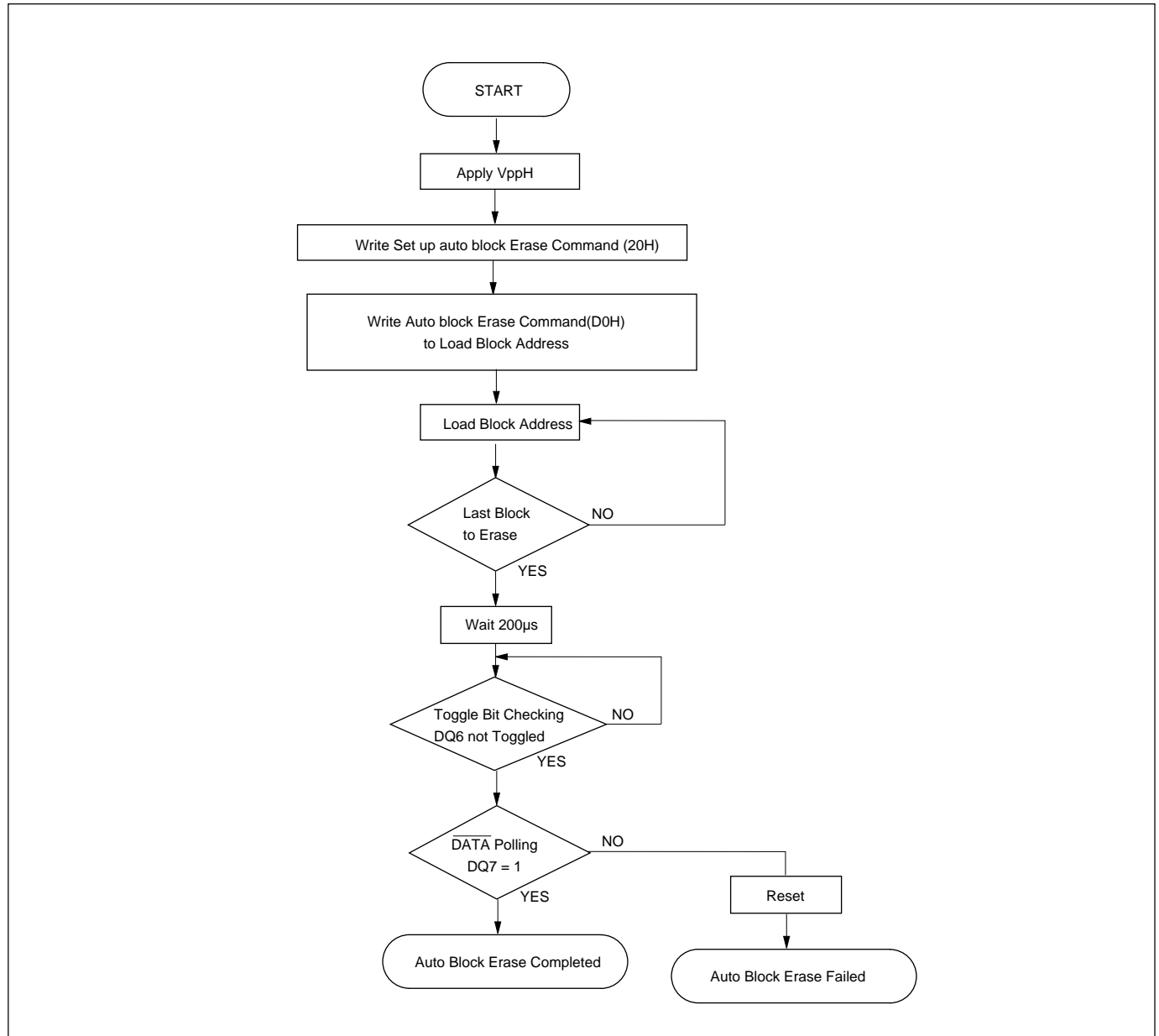
AUTOMATIC BLOCK ERASE TIMING WAVEFORM

Block data indicated by A12 to A16 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit

checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7. Q0 to Q5 (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform) are in high impedance.

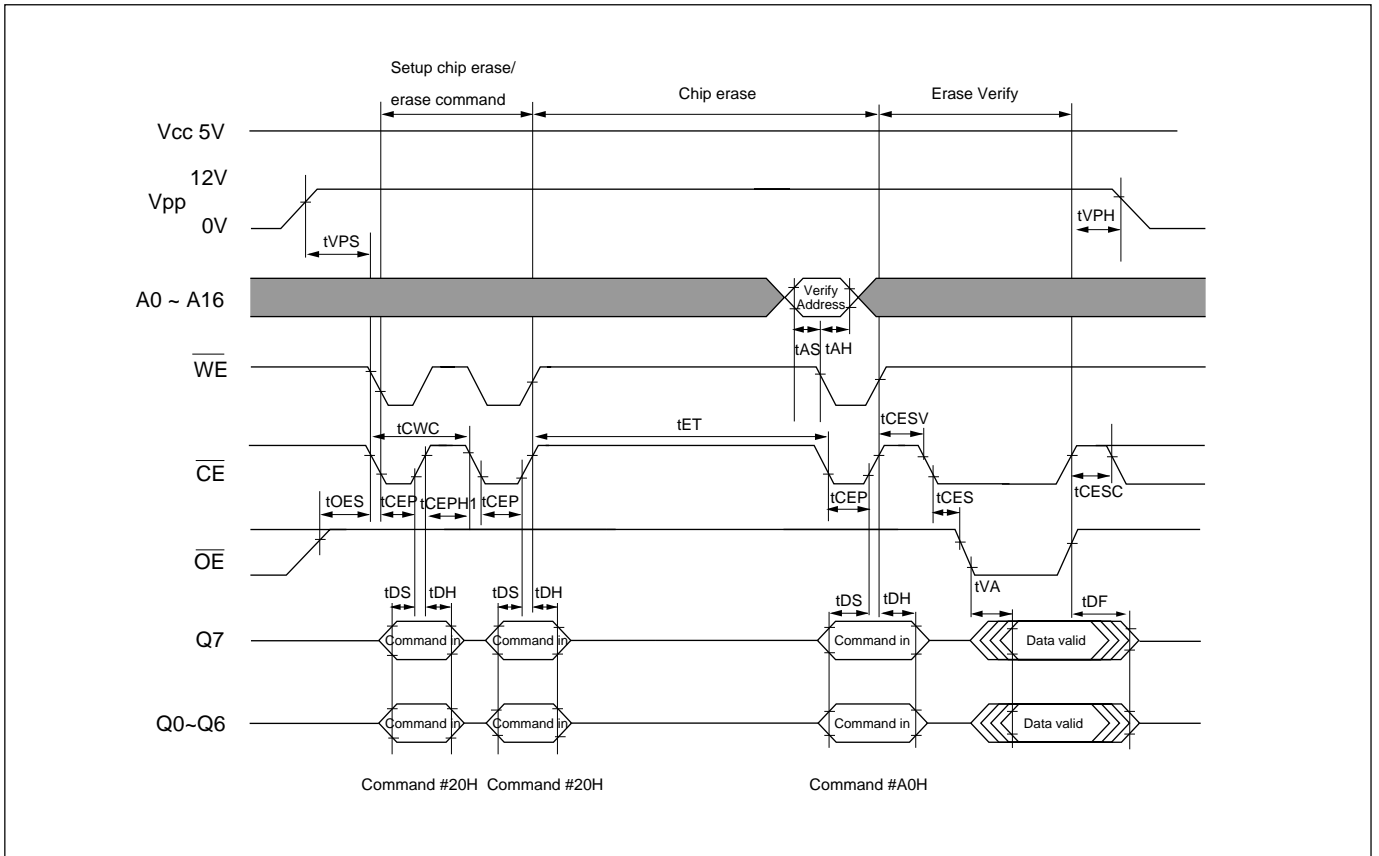


*Refer to page 2 for detailed block address.

AUTOMATIC BLOCK ERASE ALGORITHM FLOWCHART

COMPATIBLE CHIP ERASE TIMING WAVEFORM

All data in chip are erased. Control verification and additional erasure externally according to compatible chip erase flowchart.

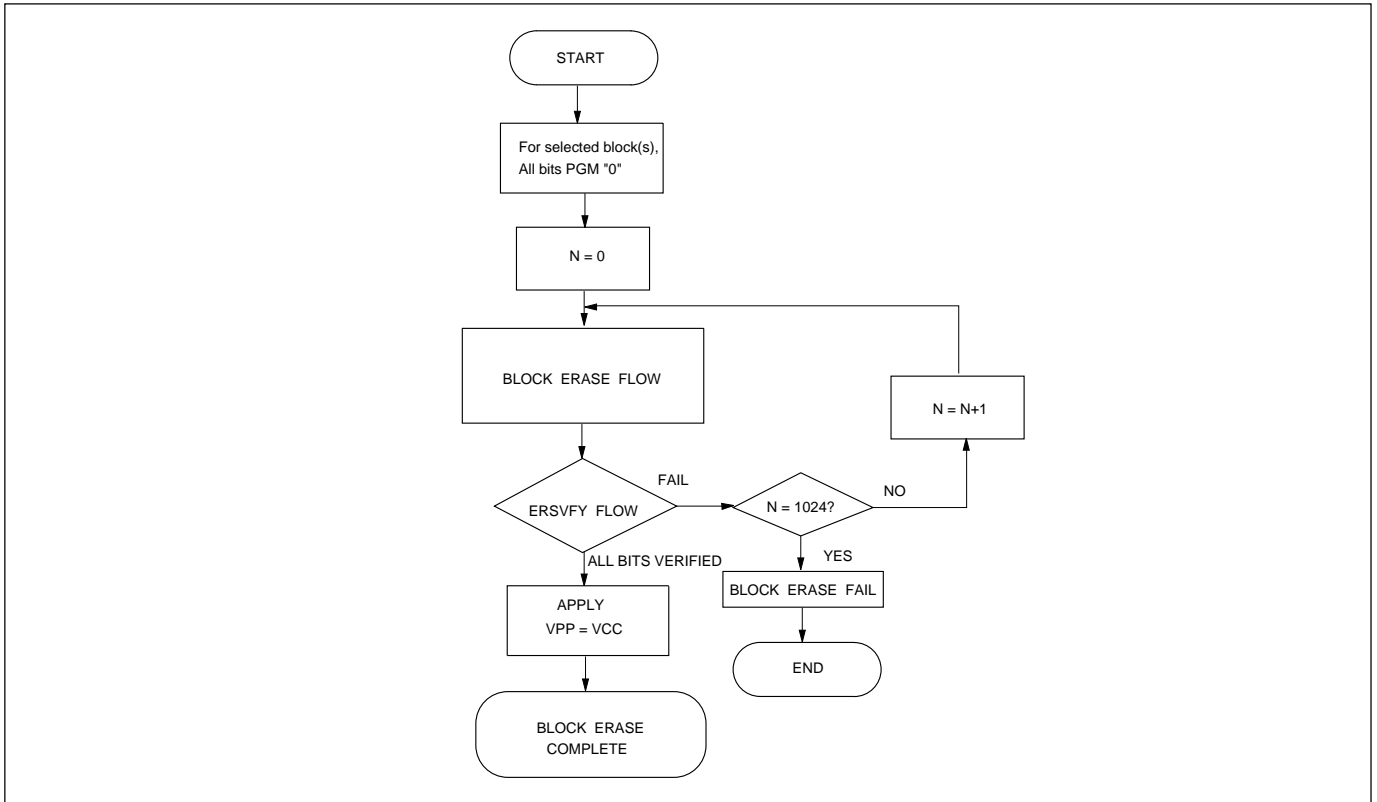


COMPATIBLE BLOCK ERASE

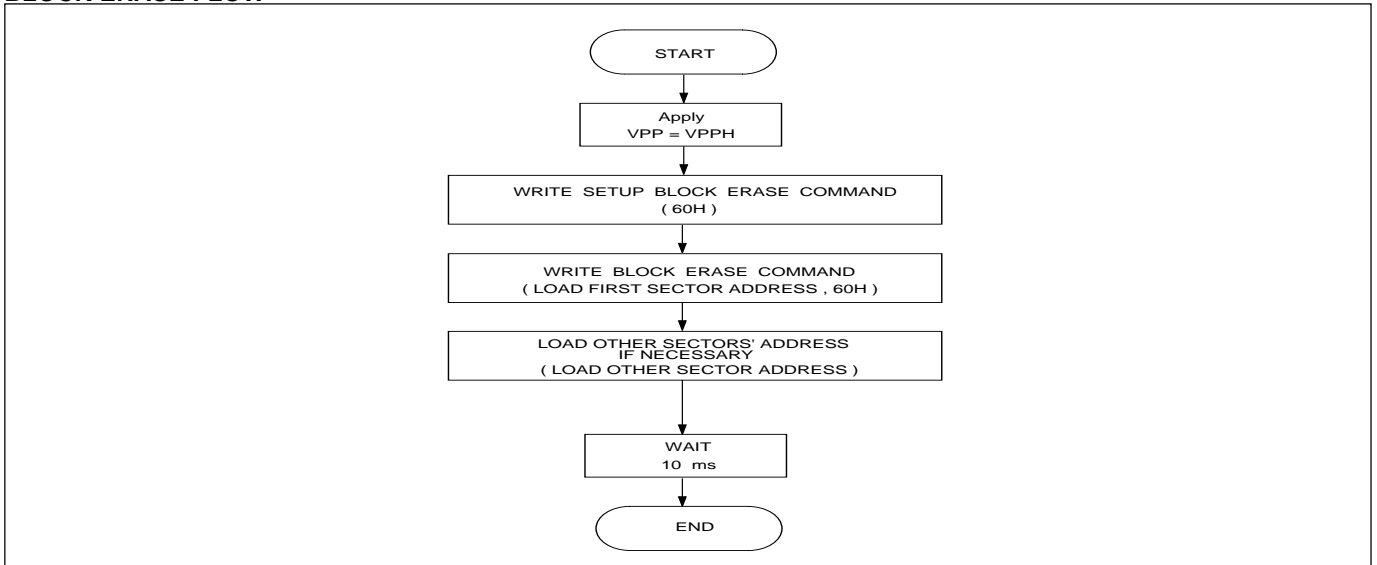
This device can be applied to the compatible block erase algorithm shown in the following flowchart. This algorithm allows to obtain faster erase time by the block (16K byte

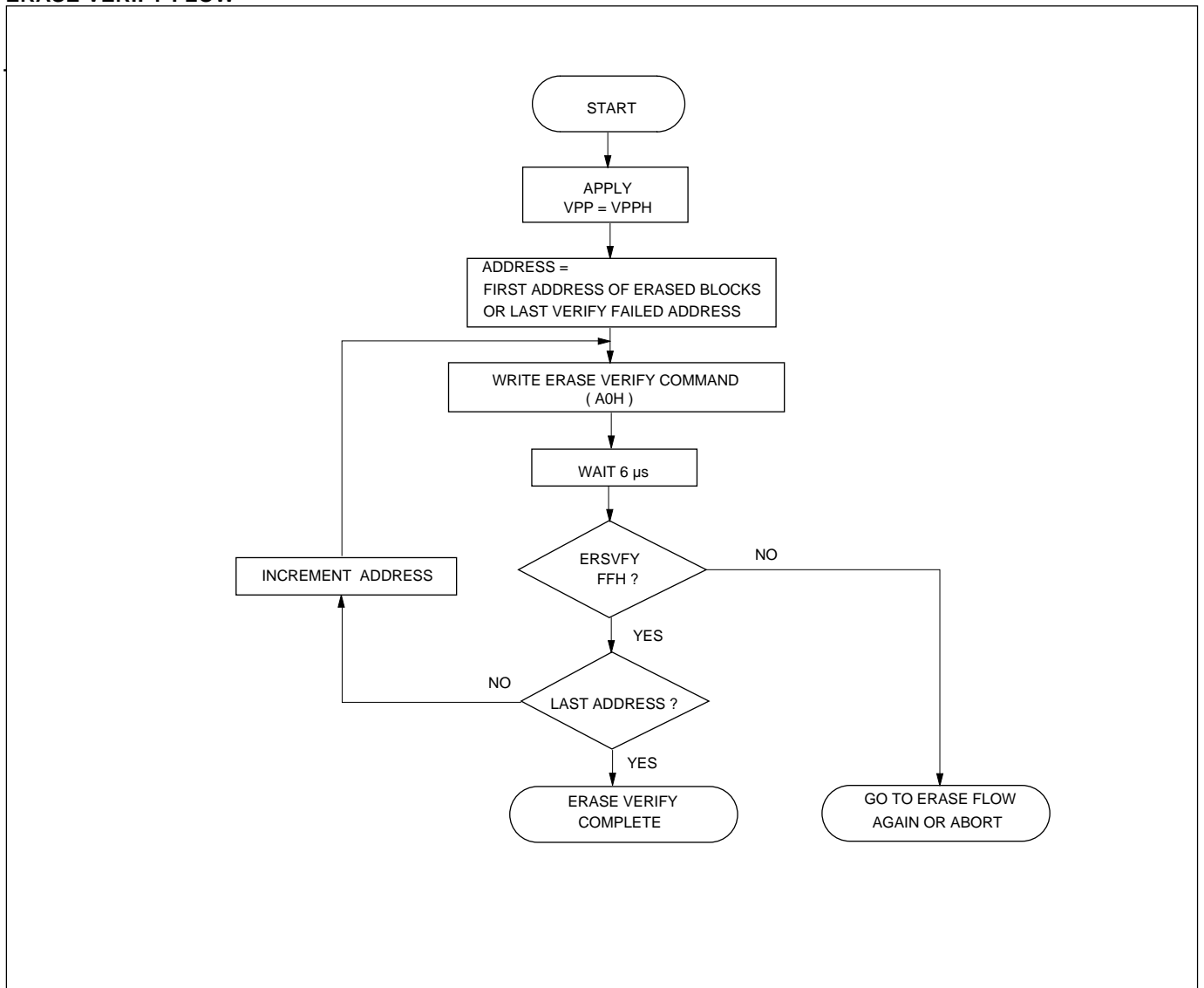
x 8 block) without any voltage stress to the device nor deterioration in reliability of data.

COMPATIBLE BLOCK ERASE FLOWCHART



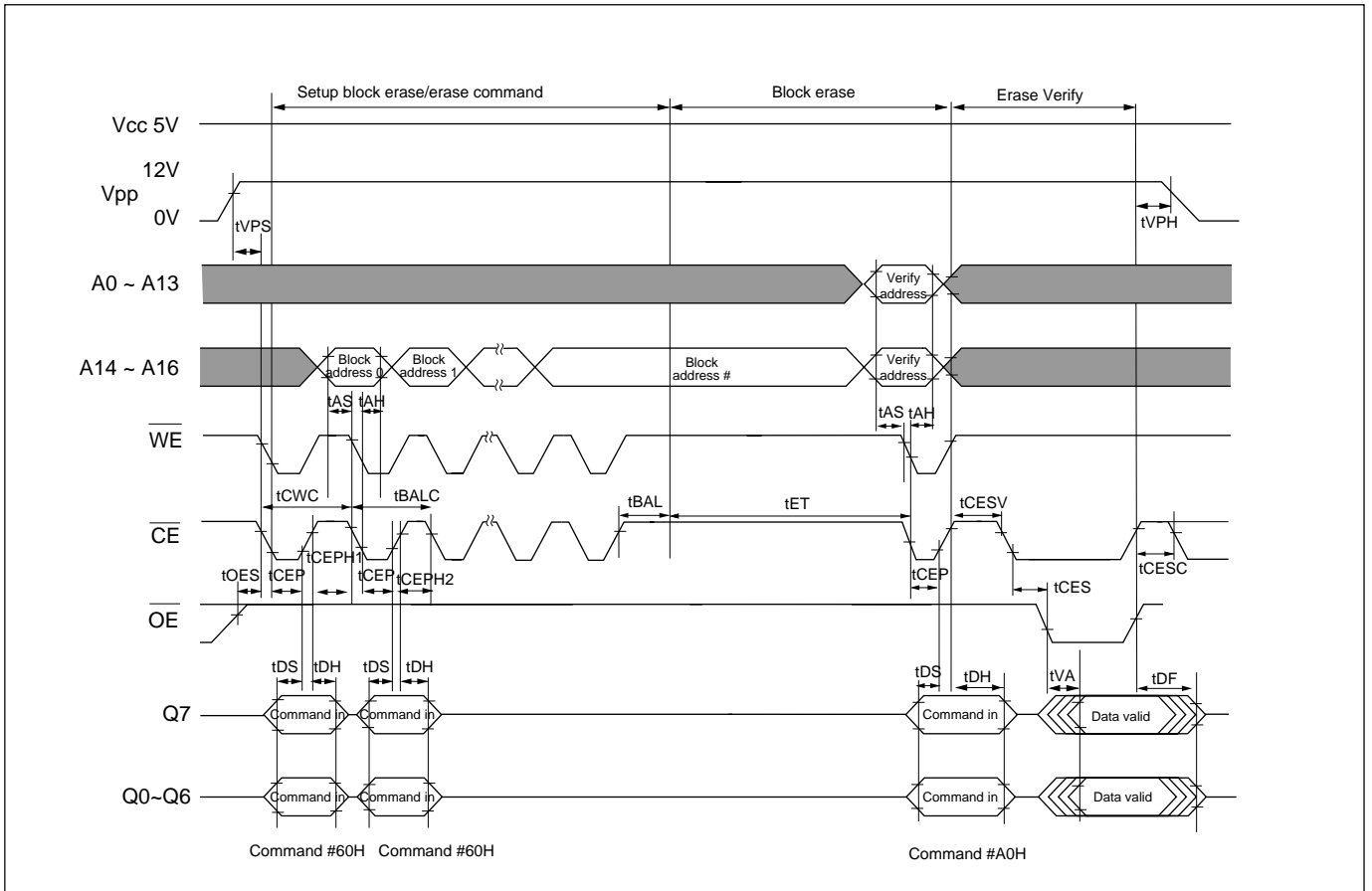
BLOCK ERASE FLOW

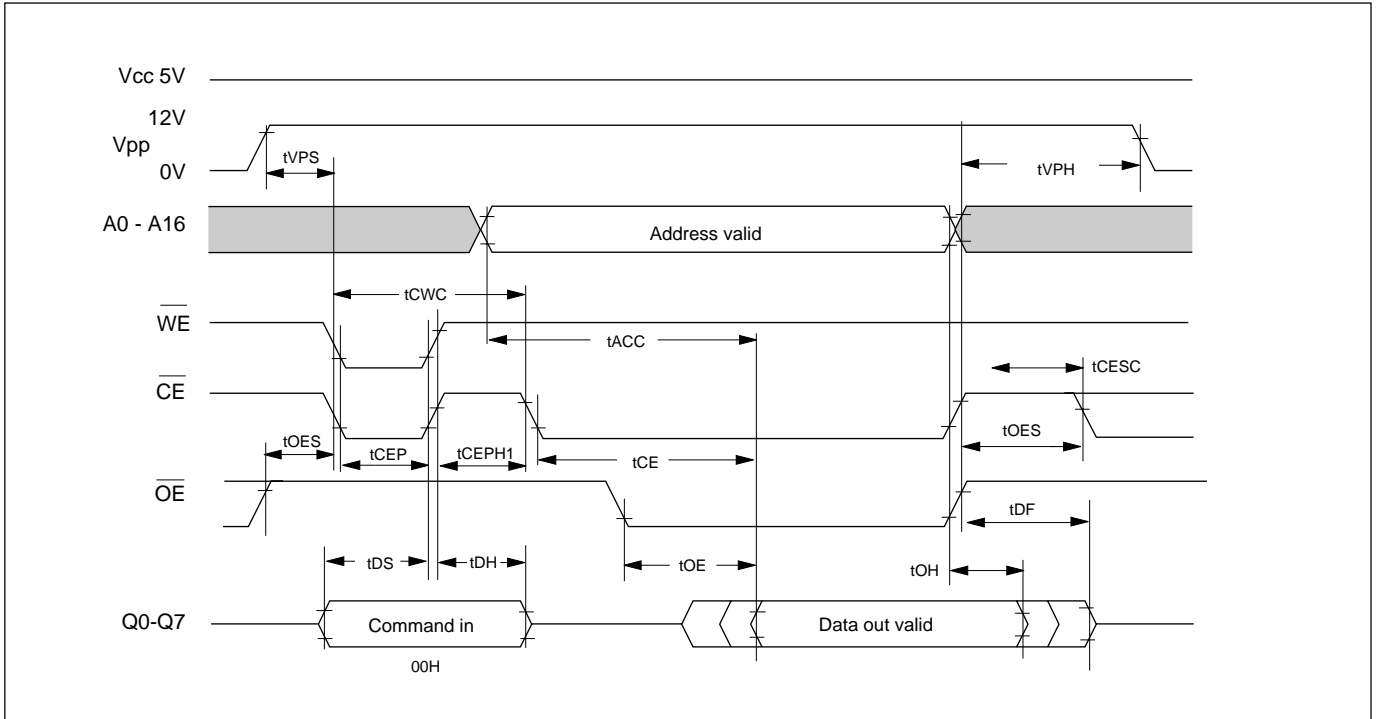
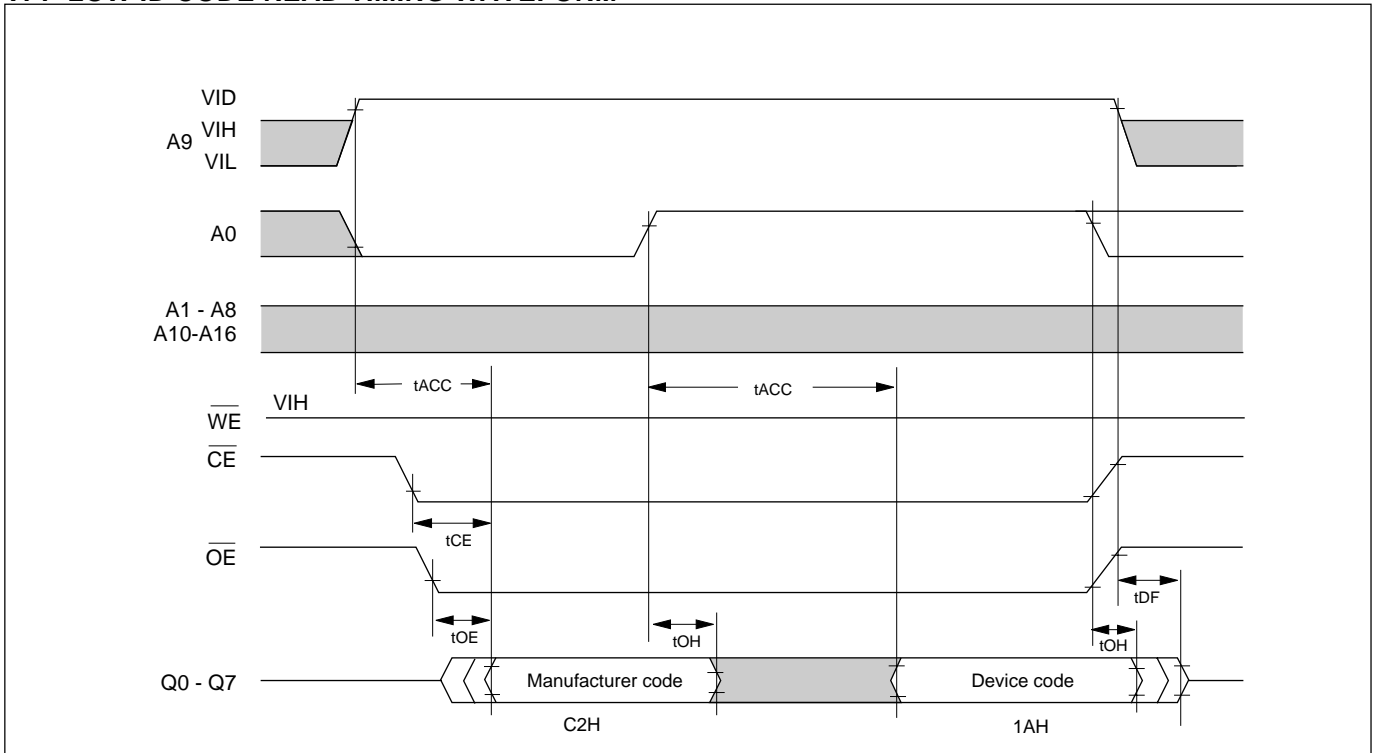


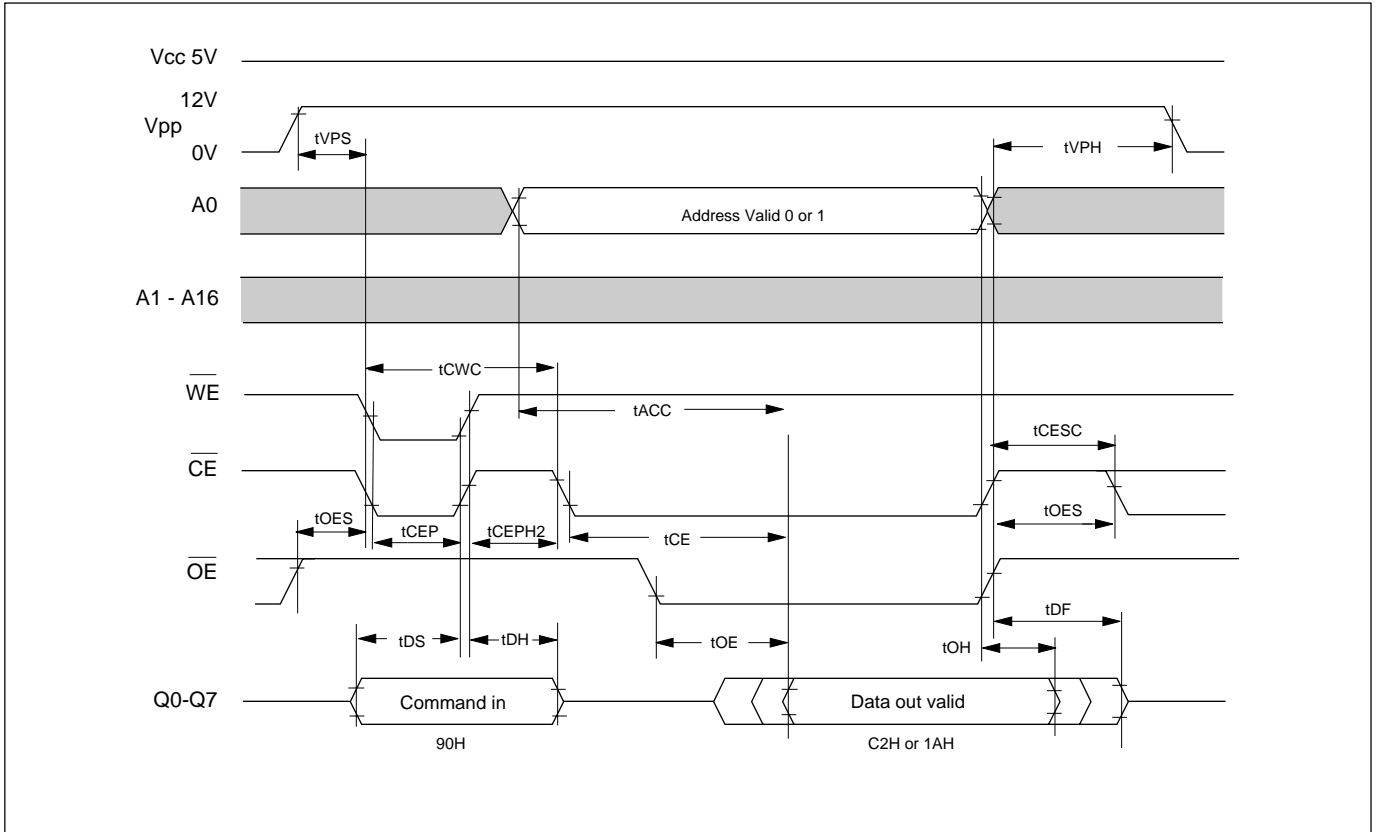
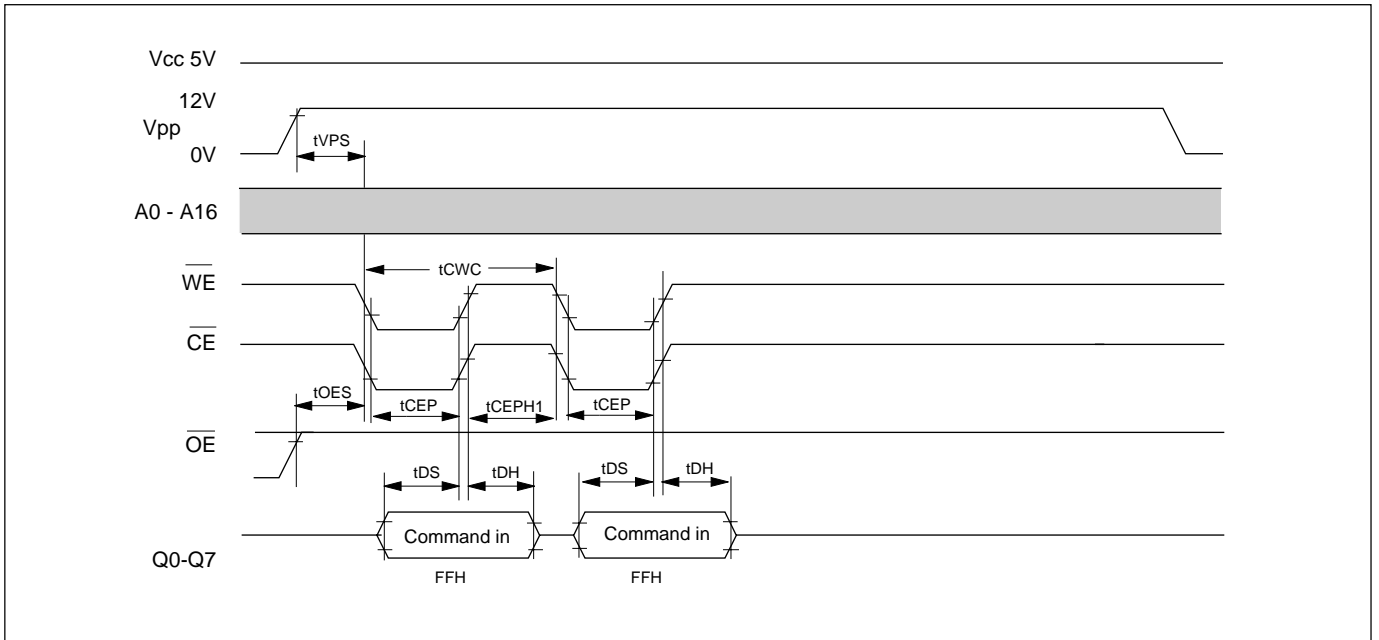
ERASE VERIFY FLOW

COMPATIBLE BLOCK ERASE TIMING WAVEFORM

Indicated block data (16 Kbyte) are erased. Control verification and additional erasure externally according to compatible block erase flowchart.

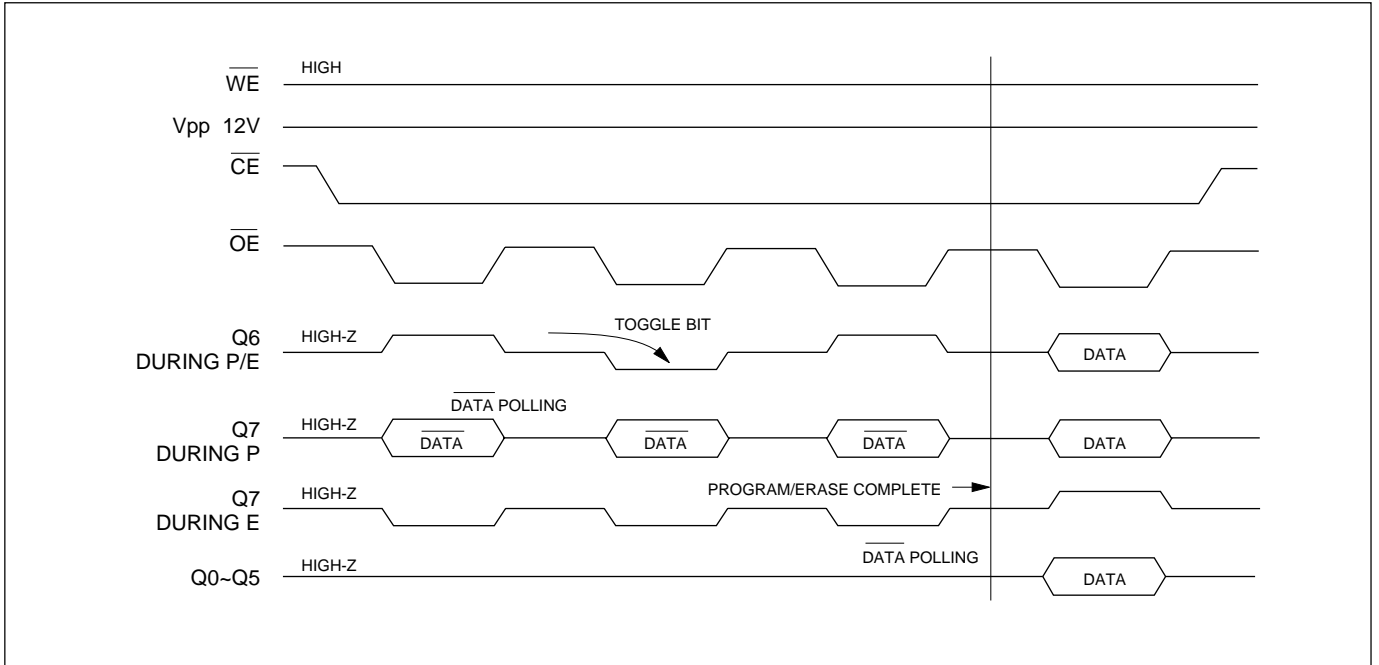


VPP HIGH READ TIMING WAVEFORM

VPP LOW ID CODE READ TIMING WAVEFORM


VPP HIGH ID CODE READ TIMING WAVEFORM

RESET TIMING WAVEFORM


TOGGLE BIT, $\overline{\text{DATA POLLING}}$ TIMING WAVEFORM

Toggle bit appears in Q6, when program/erase is operating. $\overline{\text{DATA POLLING}}$ appears in Q7 during programming or erase.



ORDERING INFORMATION PLASTIC PACKAGE

| PART NO. | ACCESS TIME | OPERATING | STANDBY | PACKAGE | ERASE/PROGRAM |
|-------------------|-------------|---------------------|---------------------|-------------------------------|---------------------|
| | (ns) | CURRENT MAX.(mA) | CURRENT MAX.(μA) | | CYCLE MIN.(time) |
| MX28F1000PPC-70C4 | 70 | 50 | 100 | 32 Pin DIP | 10,000 |
| MX28F1000PPC-90C4 | 90 | 50 | 100 | 32 Pin DIP | 10,000 |
| MX28F1000PPC-12C4 | 120 | 50 | 100 | 32 Pin DIP | 10,000 |
| MX28F1000PQC-70C4 | 70 | 50 | 100 | 32 Pin PLCC | 10,000 |
| MX28F1000PQC-90C4 | 90 | 50 | 100 | 32 Pin PLCC | 10,000 |
| MX28F1000PQC-12C4 | 120 | 50 | 100 | 32 Pin PLCC | 10,000 |
| MX28F1000PTC-70C4 | 70 | 50 | 100 | 32 Pin TSOP (Normal Type) | 10,000 |
| MX28F1000PTC-90C4 | 90 | 50 | 100 | 32 Pin TSOP (Normal Type) | 10,000 |
| MX28F1000PTC-12C4 | 120 | 50 | 100 | 32 Pin TSOP (Normal Type) | 10,000 |
| MX28F1000PRC-70C4 | 70 | 50 | 100 | 32 Pin TSOP (Reverse Type) | 10,000 |
| MX28F1000PRC-90C4 | 90 | 50 | 100 | 32 Pin TSOP (Reverse Type) | 10,000 |
| MX28F1000PRC-12C4 | 120 | 50 | 100 | 32 Pin TSOP (Reverse Type) | 10,000 |

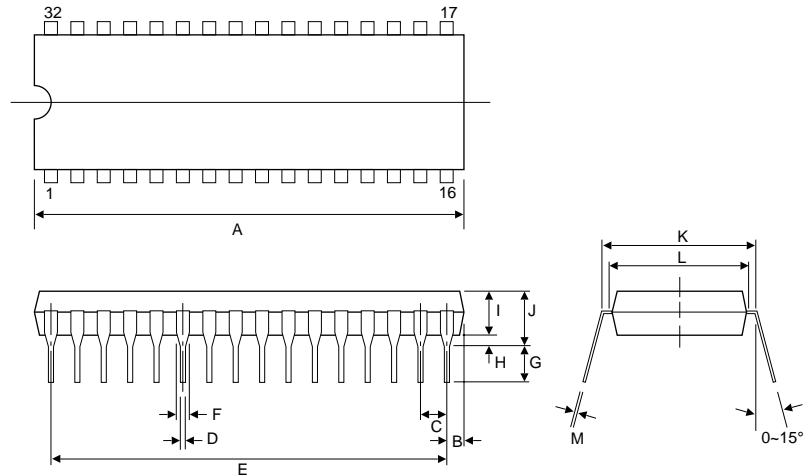
Note. Revision History

| Revision # | Description |
|------------|--|
| 1.4 | Fast access time 150ns and 1,000 times erase cycles removed. T sop pin configuration diagram rotated 180°. |
| The | flow chart of block erase corrected. |
| 1.5 | Fast access time 70ns added. |

PACKAGE INFORMATION
32-PIN PLASTIC DIP

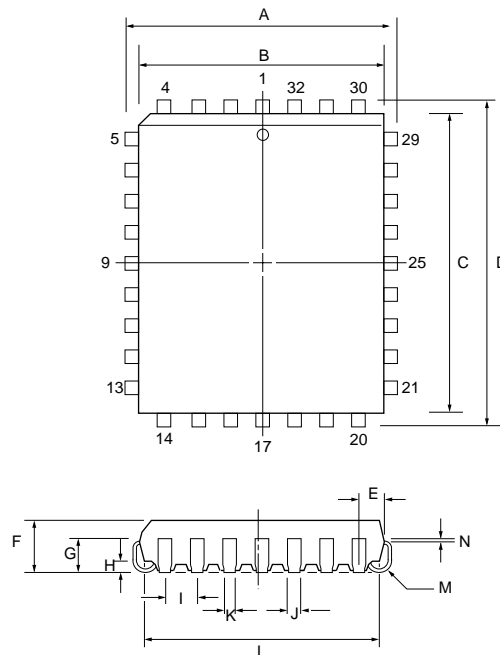
| ITEM | MILLIMETERS | INCHES |
|------|-------------|-------------|
| A | 42.13 max. | 1.660 max. |
| B | 1.90 [REF] | .075 [REF] |
| C | 2.54 [TP] | .100 [TP] |
| D | .46 [Typ.] | .050 [Typ.] |
| E | 38.07 | 1.500 |
| F | 1.27 [Typ.] | .050 [Typ.] |
| G | 3.30 ± .25 | .130 ± .010 |
| H | .51 [REF] | .020 [REF] |
| I | 3.94 ± .25 | 1.55 ± .010 |
| J | 5.33 max. | .210 max. |
| K | 15.22 ± .25 | .600 ± .101 |
| L | 13.97 ± .25 | .550 ± .010 |
| M | .25 [Typ.] | .010 [Typ.] |

NOTE: Each lead centerline is located within .25mm [.01 inch] of its true position [TP] at a maximum at maximum material condition.


32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

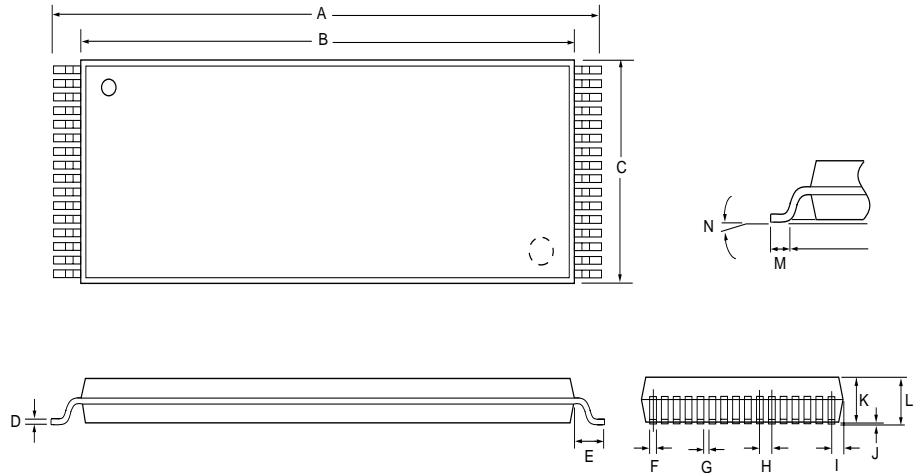
| ITEM | MILLIMETERS | INCHES |
|------|-------------|-------------|
| A | 12.44 ± .13 | .490 ± .005 |
| B | 11.50 ± .13 | .453 ± .005 |
| C | 14.04 ± .13 | .553 ± .005 |
| D | 14.98 ± .13 | .590 ± .005 |
| E | 1.93 | .076 |
| F | 3.30 ± .25 | .130 ± .010 |
| G | 2.03 ± .13 | .080 ± .005 |
| H | .51 ± .13 | .020 ± .005 |
| I | 1.27 [Typ.] | .050 [Typ.] |
| J | .71 [REF] | .028 [REF] |
| K | .46 [REF] | .018 [REF] |
| L | 10.40/12.94 | .410/.510 |
| | (W) (L) | (W) (L) |
| M | .89R | .035R |
| N | .25 [Typ.] | .010 [Typ.] |

NOTE: Each lead centerline is located within .25mm [.01 inch] of its true position [TP] at a maximum at maximum material condition.



32-PIN PLASTIC TSOP

| ITEM | MILLIMETERS | INCHES |
|------|-------------|-------------|
| A | 20.0 ± .20 | .078 ± .006 |
| B | 18.40 ± .10 | .724 ± .004 |
| C | 8.20 max. | .323 max. |
| D | 0.15 [Typ.] | .006 [Typ.] |
| E | .80 [Typ.] | .031 [Typ.] |
| F | .20 ± .10 | .008 ± .004 |
| G | .30 ± .10 | .012 ± .004 |
| H | .50 [Typ.] | .020 [Typ.] |
| I | .45 max. | .018 max. |
| J | 0 ~ .20 | 0 ~ .008 |
| K | 1.00 ± .10 | .039 ± .004 |
| L | 1.27 max. | .050 max. |
| M | .50 | .020 |
| N | 0 ~ 5° | .500 |



NOTE: Each lead centerline is located within .25mm [.01 inch] of its true position [TP] at a maximum at maximum material condition.

MACRONIX INTERNATIONAL CO., LTD

HEADQUARTERS :

TEL : +886-3-578-8888
 FAX : +886-3-578-8887

EUROPE OFFICE :

TEL : +32-2-456-8020
 FAX : +32-2-456-8021

JAPAN OFFICE :

TEL : +81-44-246-9100
 FAX : +81-44-246-9105

SINGAPORE OFFICE :

TEL : +65-747-2309
 FAX : +65-748-4090

TAIPEI OFFICE :

TEL : +886-2-2509-3300
 FAX : +886-2-2509-2200

MACRONIX AMERICA INC.

TEL : +1-408-453-8088
 FAX : +1-408-453-8488

CHICAGO OFFICE :

TEL : +1-847-963-1900
 FAX : +1-847-963-1909

[http : //www.macronix.com](http://www.macronix.com)