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IN DIGITAL VLSI PROCESSES
FOR ANALOG DESIGN
MODELING OF ACCUMULATION MOS CAPACITORS
Conclusions •
Measurement Results and Discussion •
The polysilicon gate depletion effect •
Model Implementation •
The two terminal MOS structure in accumulation •
Introduction •

Outline
(4 metal layers).

Metal-metal edge capacitors have densities of about 0.5 \( \text{ff/m}^2 \)
\[ C' \approx \frac{x_0}{x} 7.5 \text{ ff/m}^2 \]

For example, in a 0.25 \( \text{um} \) CMOS process

- Two terminal MOS capacitor.
- Alternative is to use the "flat" parts of the C-V curve of a MOS structure.
- Metal-metal structures have very low specific capacitance.
- Digital CMOS technologies.
- High density poly-poly capacitors are not available in low cost.

INTRODUCTION
OTHER BENEFITS OF MOS CAPACITORS

Example: Parasitics match integrating capacitors in filters

More accurate capacitor ratios because the integrating capacitors and parasitics track over process and temperature (useful in continuous-time filters)
MOS CAPACITOR STRUCTURES IN \textit{n}-WELL CMOS PROCESSES

- \textbf{(a) Accumulation}

- \textbf{(b) Inversion}
Existing SPICE models totally inadequate in acummulation.

Curately modeled.

For analog design, derivatives of the C-V curve must be ac-
mulation is preferable to operation in inversion.

It has been shown (by Bear et al) that operation in ac-

MOTIVATION
THE POLY-n-WELL MOS CAPACITOR

In accumulation, holes in the n-well can be neglected.
An explicit model would be more convenient.

\[(3) \quad \frac{\partial C + x_0 \partial C}{\partial C x_0 \partial C} = q^6_i C\]

Use \(q^6_i C\) in the following to get

\[(2) \quad \frac{i \phi - s \phi - \left(\frac{i \phi}{s \phi}\right) \exp x_0 \phi}{(I - (\frac{i \phi}{s \phi}) \exp x_0 \phi)} = i \partial C\]

Use the obtained above in the following to get \(i \partial C\)

\[(1) \quad \frac{i \phi - s \phi - \left(\frac{i \phi}{s \phi}\right) \exp x_0 \phi}{(I + s \phi + \exp B \Lambda = B \exp B \Lambda}\]

For a given \(\Lambda \exp B\), solve for the equation \(s \phi\)

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Calculating \(q^6_i C\)
Using this, the capacitance of the structure can be calculated.

\[
\left( \frac{\frac{\phi \gamma}{\varepsilon_0} + 1}{\frac{\phi \varepsilon_0}{\varepsilon_0} + \frac{\gamma B}{\varepsilon_0} - \frac{\gamma B}{\varepsilon_0}} \right) \log \left[ \frac{\phi \varepsilon_0 + \frac{\gamma B}{\varepsilon_0} - \frac{\gamma B}{\varepsilon_0}}{\phi \varepsilon_0 + \frac{\gamma B}{\varepsilon_0} - \frac{\gamma B}{\varepsilon_0}} \right] \phi Z = s \phi
\]

It can be shown that an approximate explicit expression for the surface potential is:

\[
\text{AN EXPLICIT EXPRESSION FOR THE SURFACE POTENTIAL}
\]
MODEL VALIDATION

Comparison of numerical simulation and proposed models for changes in substrate doping concentrations (− numerical, ⊕ proposed).

\[ C'_{ox} = 3.84 \text{ fF/\mu m}^2, \; V_{FB} = 0, \; T=300 \text{ K}. \]
MODEL VALIDATION

Variation of Capacitance with Temperature (− numerical, + proposed).

\[ C'_{\text{ox}} = 3.84 \text{ fF/\mu m}^2, \quad V_{FB} = 0, \quad N_D = 10^{17} \text{ cm}^{-3}. \]
(6) \[ (S \Phi - s \Phi - B \Xi \Lambda)^{x_0 \rho} = x_0 \Phi^{x_0 \rho} = \rho \rho \]

(5) \[ \rho \rho - \Phi - s \Phi - (\frac{\Phi}{s \Phi}) \exp \Phi \sqrt{B N^{s \Phi 2 \Phi}} = \rho \rho - \rho \rho = \rho \rho \]

There are 2 ways of doing this.

TRAN analysis is needed.

MODEL IMPLEMENTATION IN SPICE
DISTORTION COMPARISON WITH A FINELY SPACED PWL DATA FROM DEVICE SIMULATION

Second harmonic relative to fundamental (− PWL, ⊕ proposed)
DISTORTION COMPARISON WITH A FINELY SPACED PWL DATA FROM DEVICE SIMULATION

Third harmonic relative to fundamental (− PWL, ⊕ proposed)
CIRCUIT CONSIDERATIONS AND CHOICE OF POLYSILICON TYPE

For circuit work, we need the structure to be in strong accumulation for as low a bias voltage as possible $\Rightarrow V_{FB}$ should be as negative as possible $\Rightarrow$ Use n-type polysilicon.
The Polysilicon Gate Depletion Effect

- It is not possible to dope the gate infinitely high with donors.

- Finite doping levels in the gate cause a thin gate depletion layer.
(6) \[ \frac{x^0_C}{\frac{\lambda T \text{Pol}}{\sqrt{2} g_e s N}} = d_j \]

where

(8) \[ \frac{(s \phi - M W \phi - B C I)}{x^0_C} \approx d_{eq} C \]

(7) \[ \frac{d_{eq} C}{I} + \frac{C}{I} + \frac{x^0 C}{I} = \frac{q C}{I} \]

The capacitance of this layer appears in series with \( C \) and \( x^0 \).

The Polysilicon Gate Depletion Effect
Comparison for a 84 Å gate oxide capacitor (–model, ☻ data).
Comparison for a 45 Å gate oxide capacitor (−model, ⊕ data).
The model has been implemented in SPICE.

• analog design.

The model accurately predicts distortion, which is useful in

into the model.

The polysilicon gate depletion effect has been incorporated in

accumulation.

An explicit model has been proposed for a MOS capacitor in

CONCLUSIONS