DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD7225

PROGRAMMABLE LCD CONTROLLER/DRIVER

The μPD7225 is a software-programmable LCD (Liquid Crystal Display) controller/driver. The μPD7225 can be serially interfaced with the CPU in a microcomputer and can directly drive 2, 3, or 4-time division LCD. The μPD7225 contains a segment decoder which can generate specific segment patterns. In addition, the μPD7225 can be used to control on/off (blinking) operation of a display.

FEATURES

- Can directly drive LCD
- Programmable time-division multiplexing
  - Static drive
  - Divide-by-2, 3, or -4 time division multiplexing
- Number of digits displayed
  - 7-segment
    Divide-by-4 time division..... 16 digits
    Divide-by-3 time division..... 10 2/3 digits
    Divide-by-2 time division..... 8 digits
    Static ..... 4 digits
  - 14-segment
    Divide-by-4 time division..... 8 digits
- Bias method
  Static, 1/2, 1/3
- Segment decoder output
  - 7-segment : Numeric characters 0 to 9, six symbols
  - 14-segment: 36 alphanumeric characters, 13 symbols
- Blinking operation
- Multi-chip configuration possible
- 8-bit serials interface
  75X series and 78K series compatible
- CMOS
- Single power supply

ORDERING INFORMATION

Part Number	Package	Quality level
μPD7225G00	52-pin plastic QFP (bend)	Standard (for general electrics application)
μPD7225G01	52-pin plastic QFP (straight)	Standard (for general electrics application)
μPD7225GB-3B7	56-pin plastic QFP (bend)	Standard (for general electrics application)

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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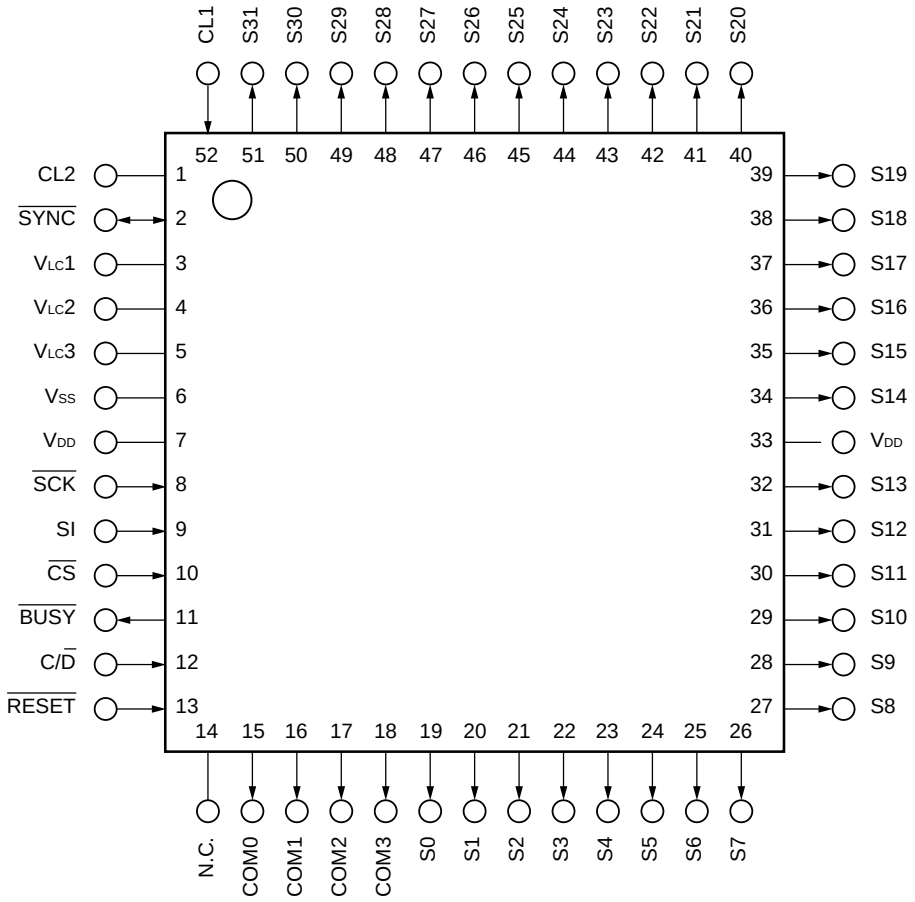
PIN CONFIGURATION: 52-pin QFP (Top View)

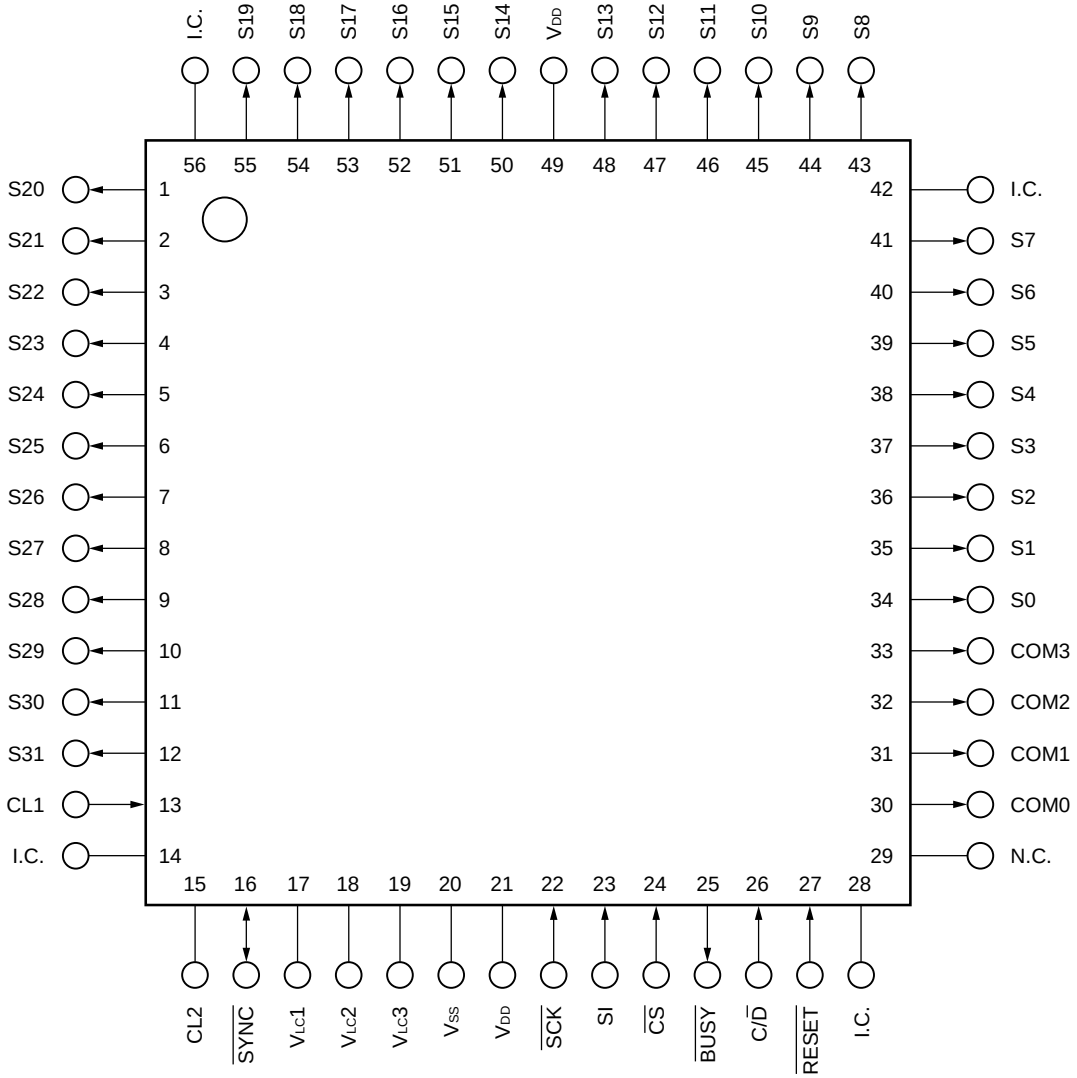
μPD7225G



SI	: Serial Input	CL1	: External Resistor 1 (External Clock)
SCK	: Serial Clock	CL2	: External Resistor 2
C/D	: Command/Data	RESET	: Reset
CS	: Chip Select	V_{LC1}-V_{LC3}	: Power Supply For LCD Drive
BUSY	: Busy	V_{DD}	:Power Supply
SYNC	: Sync	V_{SS}	: Ground
S0-S31	: Segment	I.C.	: Internally Connected
COM0-COM3	: Common		
N.C.	: Non-connection		

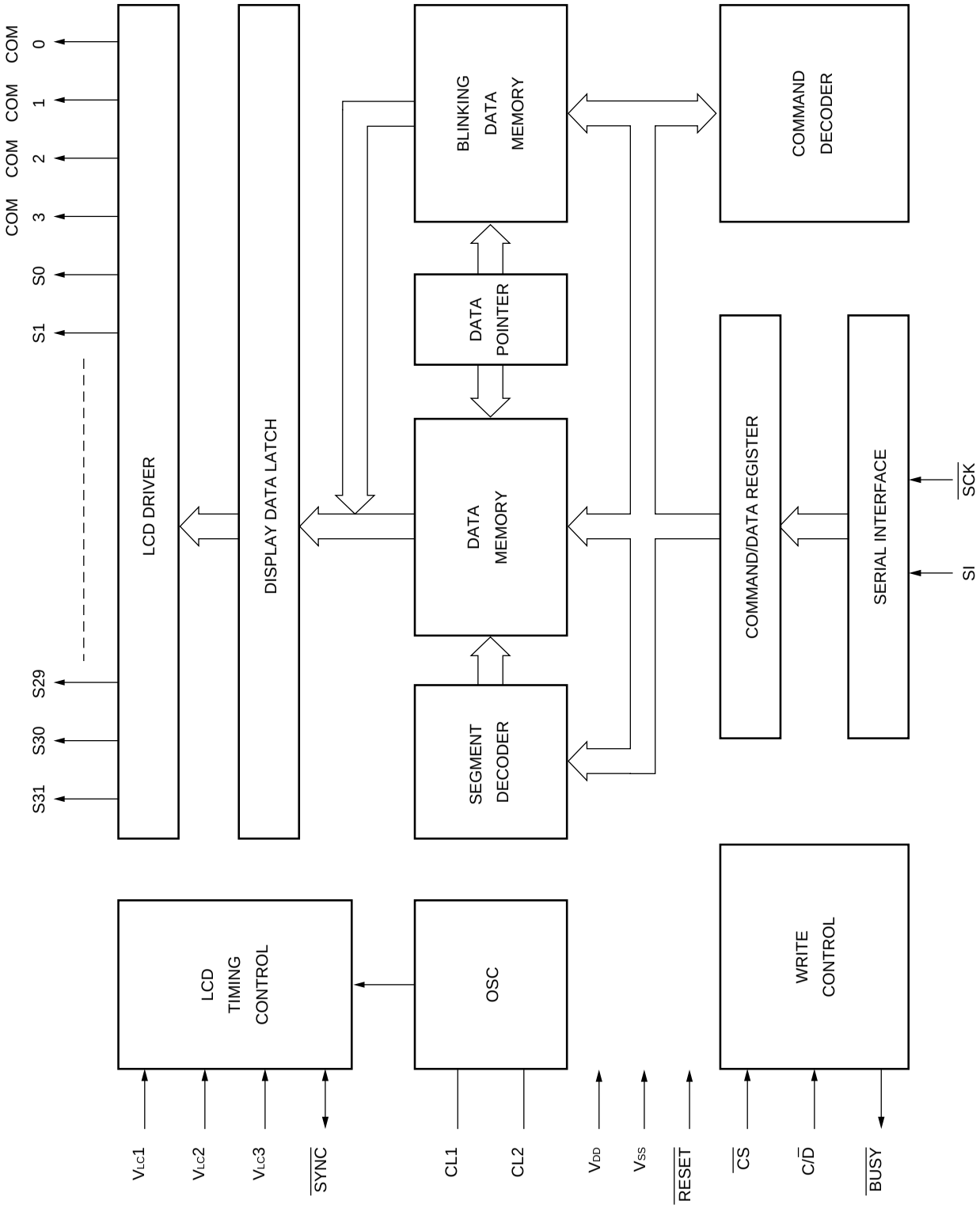
PIN CONFIGURATION: 56-pin QFP (Top View)

***μ*PD7225GB**



Note I.C. Pin must be connected to V_{DD} or left unconnected.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 SI (Serial Input)……Input

This pin is used for inputting serial data (commands/data). Data to be displayed as well as 19 deffernet commands for controlling the operation of the μPD7225 can be input to this pin.

1.2 $\overline{\text{SCK}}$ (Serial Clock)……Input

This pin is used for inputting the shift clock for serial data (SI input). The content of the SI input is read into the serial register at the rising edge of this clock one bit at a time. $\overline{\text{SCK}}$ input is effective when $\overline{\text{CS}}$ = 0 and $\overline{\text{BUSY}}$ = 1. If $\overline{\text{BUSY}}$ = 0, this input is ignored. If $\overline{\text{CS}}$ = 1, this signal is ignored regardless of the $\overline{\text{BUSY}}$ status.

1.3 C/$\overline{\text{D}}$ (Command/Data)……Input

This input indicates whether the signal input from the SI pin is a command or data. A low level indicates data; a high level indicates a command.

1.4 $\overline{\text{BUSY}}$……Tri-state output

This is an active-low output pin that is used to control serial data input disable/enable. A low level disables serial data input; a high level enables serial data input. This pin becomes high impedance when $\overline{\text{CS}}$ = 1.

1.5 $\overline{\text{CS}}$ (Chip Select)……Input

When $\overline{\text{CS}}$ is changed from high level to low level, the SCK counter in the μPD7225 is cleared and serial data input is enabled. At the same time, the data pointer is initialized to address 0. When $\overline{\text{CS}}$ is set to high level after serial data is input, the contents of the data memory are trnasferred to the display latch and displayed on the LCD.

1.6 $\overline{\text{SYNC}}$ (SYNChronous)……Input/Output

The $\overline{\text{SYNC}}$ pin is used to make a wired OR connection when the common pins are shared or when blinking operation is synchronized in a multi-chip configuration.

When the μPD7225 is reset ($\overline{\text{RESET}}$ = 0), the $\overline{\text{SYNC}}$ pin outputs the clock frequency (f_{CL}) divided by four (refer to Figure 1), and synchronizes the system clock (f_{CL}/4) of the μPD7225. When the reset is released ($\overline{\text{RESET}}$ =1), the display timing of each μPD7225 is synchronized with the common drive signal timing shown in Figure 2.

Figure 1. $\overline{\text{SYNC}}$ Pin Status During Reset ($\overline{\text{RESET}}$ = 0)

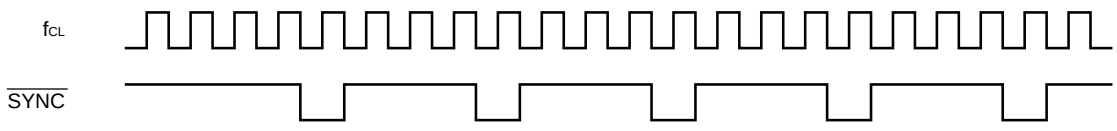
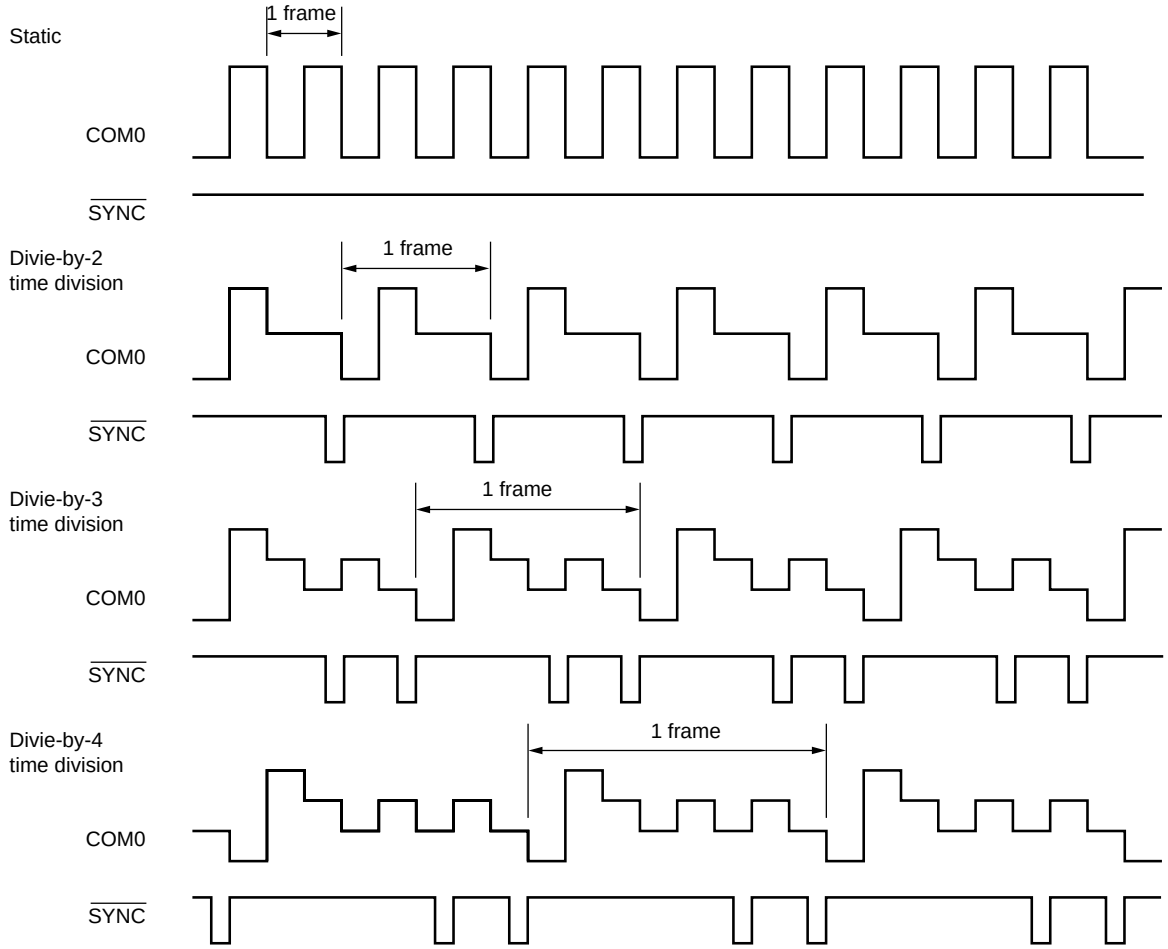


Figure 2. $\overline{\text{SYNC}}$ Pin Status after Reset ($\overline{\text{RESET}}$ = 1)



1.7 $\overline{\text{RESET}}$……Input

This is an active low reset input pin.

1.8 S0-S31 (Segment)……Output

These pins output segment drive signals.

1.9 COM0-COM3 (COMmon)……Output

These pins output common drive signals.

1.10 CL1, CL2 (Clock)

A resistor is connected across these pins for internal clock generation. When inputting an external clock, use the CL1 pin for input.

1.11 V_{LC1}, V_{LC2}, V_{LC3}

LCD driver power supply pin.

1.12 V_{DD}

Positive power supply pin. Either pin 7 or pin 33 can be used.

1.13 V_{SS}

GND pin.

2. INTERNAL SYSTEM CONFIGURATION

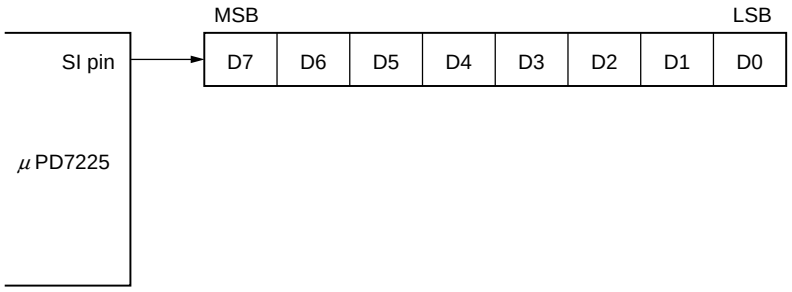
2.1 Serial Interface

The serial interface consists of an 8-bit serial register and a 3-bit SCK counter.

The serial register clocks in the serial data from the SI pin at the rising edge of $\overline{SCK}$. At the same time, the SCK counter increments (+1) the serial clock. As a result, if an overflow occurs (when eight pulses are counted), input from the SI pin is disabled ($\overline{BUSY}$ = 0), and the contents of the serial register is output to the command/data register.

The $\overline{SCK}$ should be set to high before serial data is input and after the data has been input (after eight clocks are input to $\overline{SCK}$).

Serial data must be input to the SI pin beginning with MSB first.



2.2 Command/Data Register

The command/data register latches the contents of the serial register in order to process the serial data clocked into the serial register. After the serial data is latched, if the clocked in data is specified as command, the command/data register transfers its contents to the command decoder. If specified as data the command/data register transfers its contents to data memory or the segment decoder.

2.3 Command Decoder

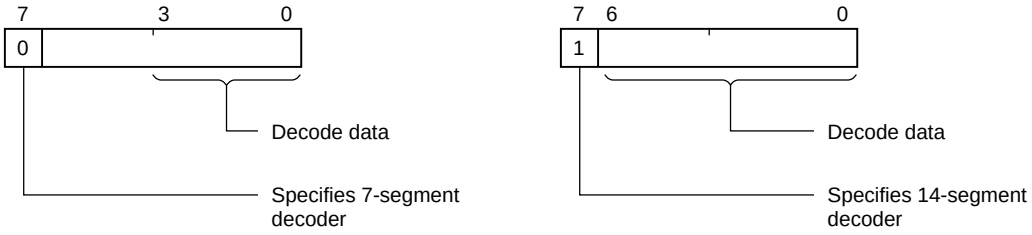
When the contents of the command/data register are specified as a command (C/$\overline{D}$ was high when data was input), the command decoder, clocks in the contents of the command/data register and controls the μPD7225.

2.4 Segment Decoders

The μPD7225 has a 7-segment decoder for use with divide-by-3 and divide-by-4 time division, and a 14-segment decoder for use divide-by-4 time division.

The 7-segment decoder can generate signals for numeric characters 0 to 9 and six different symbols. The 14-segment decoder can generate signals for 36 alphanumeric characters and 13 different symbols. When the WITH SEGMENT DECODER command is executed, if the contents of the command/data register are specified as data, the contents will be input to the segment decoder, and converted to display codes, and then automatically written to the data memory. Whether to select the 7-segment decoder or 14-segment decoder is determined by the most significant bit (bit 7) of the data input to the segment decoder. It the most significant bit is 0, the 7-segment decoder will be selected. If it is 1, the 14-segment decoder will be selected. If the 7-segment decoder is selected (however, divide-by-3 and divide-by-4 time division), the lower 4 bits (bit 3 to bit 0) of the input data (C/$\overline{D}$ = 0) will be decoded and written to the data memory.

If the 14- segment decoder is selected (however, divide-by-4 time division), the lower 7 bits of the input data (C/$\overline{D}$ = 0) will be decoded and written to the data memory.

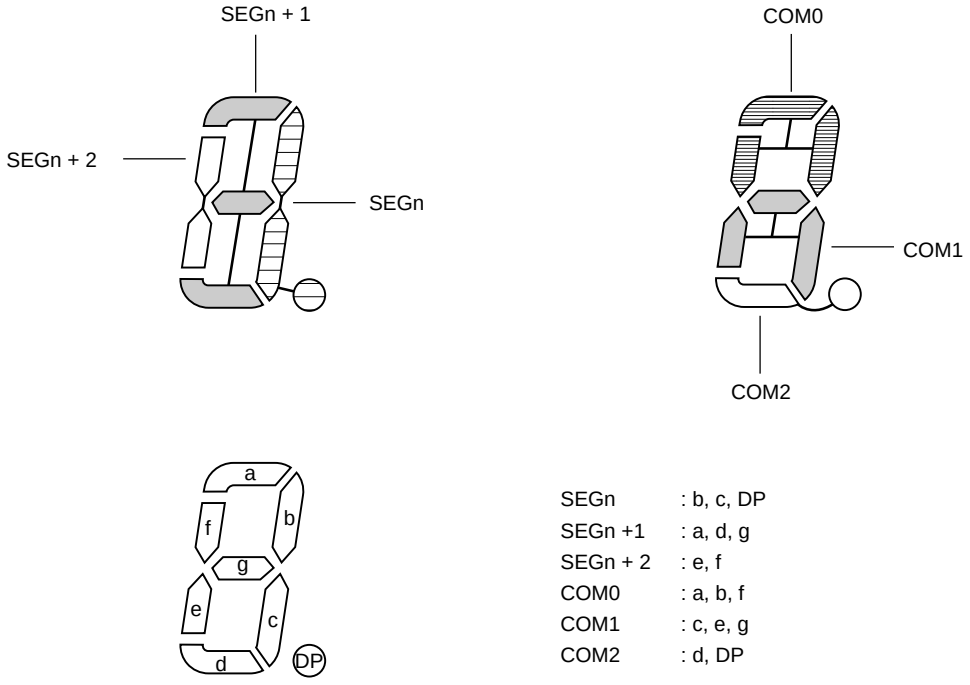


When displaying the output of the segment decoder (display data) on the LCD, use an LCD configured as shown in Figure 3 or Figure 4.

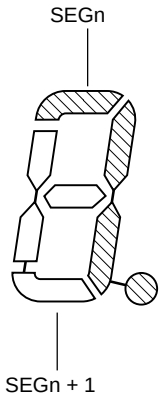
If another type of LCD is used, the displayed pattern will be different.

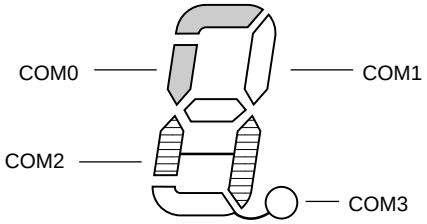
Figure 3. 7-Segment Type LCD

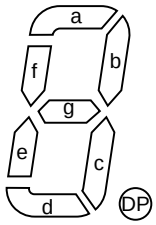
When configuring the LCD for divide-by-3 time division mode, connect as follows:



When configuring the LCD for divide-by-4 time division mode, connect as follows:



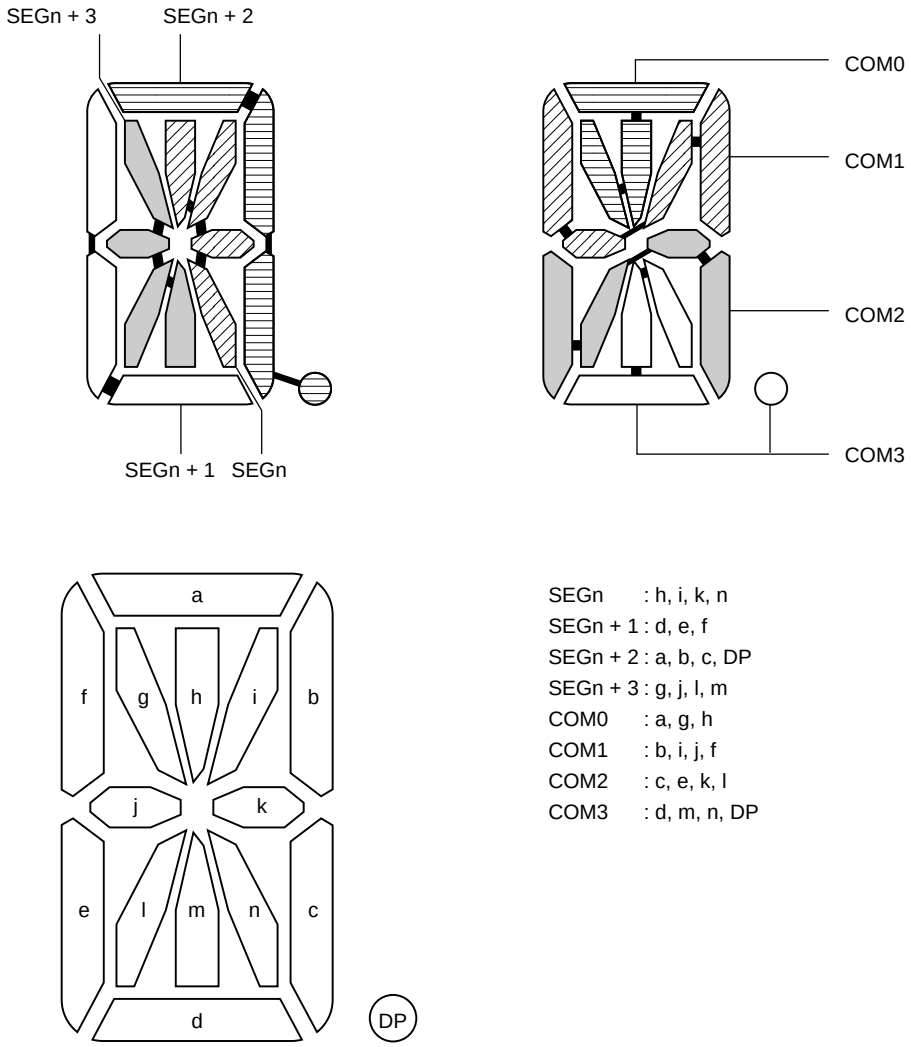




SEGn : a, b, c, DP
SEGn + 1 : d, e, f, g
COM0 : a, f
COM1 : b, g
COM2 : c, e
COM3 : d, DP

Figure 4. 14-Segment LCD

The 14-segment type LCD can be used only in the divide-by-4 time division mode. For the 14-segment LCD type, connect segments and commons as follows:



The following shows the input data and display pattern, and the configuration of the display data which is automatically written into the data memory. For the 7-segment type, the lower 4 bits (D3 to D0) are decoded. For the 14-segment type, the input data and display pattern correspond to 8-bit ASCII code. The first address to which the display data is written is indicated as address N.

Figure 5. 7-Segment LCD

Data (HEX)	Display pattern	Data memory				
		Divide-by-3 time division			Divide-by-4 time division	
		N +2	N +1	N	N +1	N
00		3	5	3	D	7
01		0	0	3	0	6
02		2	7	1	E	3
03		0	7	3	A	7
04		1	2	3	3	6
05		1	7	2	B	5
06		3	7	2	F	5
07		0	1	3	0	7

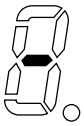
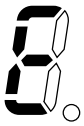
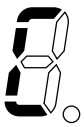
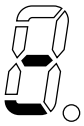
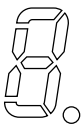
Data (HEX)	Display pattern	Data memory				
		Divide-by-3 time division			Divide-by-4 time division	
		N +2	N +1	N	N +1	N
08		3	7	3	F	7
09		1	7	3	B	7
0A		0	2	0	2	0
0B		3	7	0	F	1
0C		3	5	0	D	1
0D		0	6	0	A	0
0E		2	6	2	E	4
0F		0	0	0	0	0

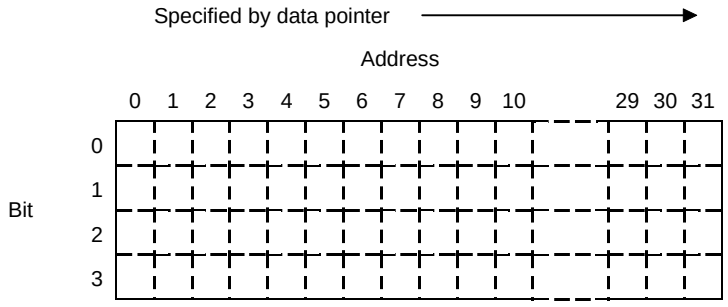
Figure 6. 14-Segment LCD

Upper bit

Lower bits	A		B		C		D	
Data (HEX)	Display pattern	Data memory N+3 N+2 N+1 N	Display pattern	Data memory N+3 N+2 N+1 N	Display pattern	Data memory N+3 N+2 N+1 N	Display pattern	Data memory N+3 N+2 N+1 N
0		0 0 0 0		4 7 E 2		A 7 C 0		2 3 6 4
1				0 6 0 0		2 7 6 4		0 7 E 8
2				2 3 C 4		8 7 8 5		2 3 6 C
3				2 7 8 4		0 1 E 0		1 5 8 4
4				2 6 2 4		8 7 8 1		8 1 0 1
5				2 5 A 4		2 1 E 4		0 6 E 0
6				2 5 E 4		2 1 6 4		4 0 6 2
7		0 0 0 2		0 7 0 0		0 5 E 4		4 6 6 8
8		0 0 0 A		2 7 E 4		2 6 6 4		5 0 0 A
9		5 0 0 0		2 7 A 4		8 1 8 1		9 0 0 2
A		F 0 0 F				0 6 C 0		4 1 8 2
B		A 0 0 5				2 0 6 A		
C				4 0 8 2		0 0 E 0		1 0 0 8
D		2 0 0 4		2 0 8 4		1 6 6 2		
E				1 0 8 8		1 6 6 8		
F		4 0 0 2				0 7 E 0		

2.5 Data Memory/Data Pointer

The data memory is a memory which stores display data (32 × 4 bits). Data input by serial transfer, command immediate data, etc., is written to the data memory.



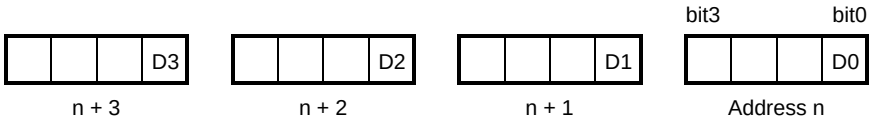
In the data memory, either data from the serial register (when the segment decoder is not used) or data from the segment decoder (when the segment decoder is used) is written as display data.

When the segment decoder is not used, all bits or the lower 4 bits of the serial data (C/$\overline{D}$ = 0) input to the serial register are assigned and written to the specific bits in location 2 to location 4 in the data memory according to the specified time division. When the segment decoder is used, the contents of the serial register (C/$\overline{D}$ = 0) are decoded by the segment decoder, and the corresponding display data are allocated to the location specified in data memory by the time division specification (devide-by-3, -4 time division) and the MSB (Most Significant Bit) of the serial data. (a) to (d) below describe these operations.

The contents of the data memory can be modified in 4-bit units or in bit units using a command.

(a) Static

The lower 4 bits of the contents of the serial register are written to bit 0 in each address (the upper 4 bits are ignored).

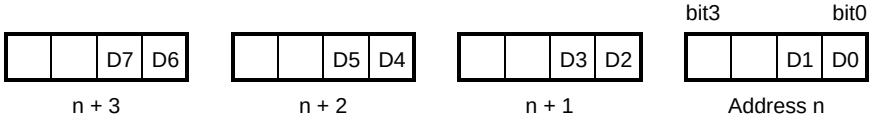


Only the content of bit 0 in each address are effective as display data.

After the data is written, the data pointer points to address n + 4.

(b) Divide-by-2 time division

The contents of the 4 even bits of the serial register are written to bit 0 in the four addresses, and the contents of 4 odd bits of the serial register are written to bit 1.

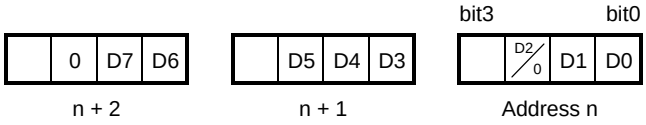


The contents of bits 0 and 1 of each address are effective as display data.

After the data is written, the data pointer points to address n + 4.

(c) Divide-by-3 time division

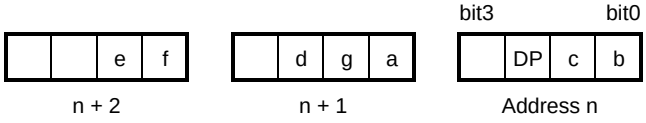
The contents of the 8 bits of the serial register of the segment decoder output (8 bits) are written to bits 0, 1, and 2 of each address. In this case, 0 will be automatically written to bit 2 of address n + 2. For segment decoder output, 0 will also be automatically written to bit 2 (D2) of address n.



The contents of bits 0, 1, and 2 of each address are effective as display data.

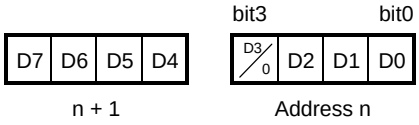
After the data is written, the data pointer points to address n + 3.

The segment decoder output written to the data memory corresponds to segments (a to g, DP) shown in Figure 3 as follows:



(d) Divide-by-4 time division

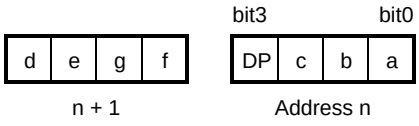
The contents of the 8 bits of the serial register or the segment decoder output (8 bits) are written to bits 0, 1, 2, and 3 of each address. For segment decoder output, 0 is automatically written to bit 3 (D3) of address n.



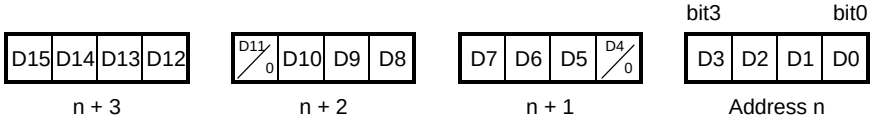
The contents of all bits of each address are effective as display data.

After the data is written, the data pointer points to address n + 2.

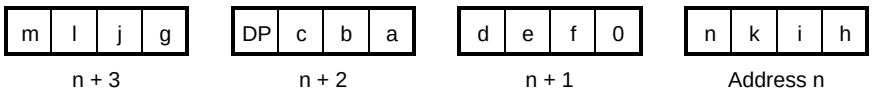
When 7 segments are used, the segment decoder output written to the data memory corresponds to segments (a to g, DP) shown in Figure 3 as follows:



When 14 segments are used, the segment decoder output is written to bits 0, 1, 2, and 3 of each address. In this case, 0s are automatically written to bit 3 of address n + 2, and bit 0 of address n+ 1.

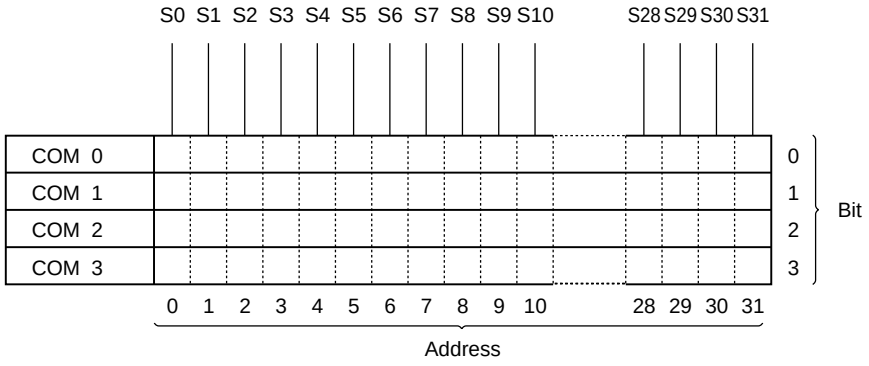


All bits of each address are effective. After the data is written, the data pointer points to address n + 4.
The segment decoder output written to the data memory corresponds to segments (a to n, DP) shown in Figure 4 as follows:

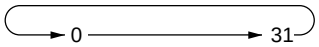


All contents of the 32 × 4-bit data memory are transferred to the 32 × 4-bit display data latch when the $\overline{CS}$ is set to high. In this case, if the DISPLAY ON command has been set, the contents of the display data latch are converted to the segment drive signal in 32-bit units in synchronization with COM0-COM3 signals, and output from the segment pins.
The figure below shows the relationship of the data memory, segment pins, and common signal selection timing.

Figure 7. Data Memory, Segment Pins, and Common Signal Selection Timing



The data pointer (5 bits) specifies the address (0-31) of the data memory to which the display data will be written (at the same time, the data pointer specifies the blinking data memory address (0-31)). The LOAD DATA POINTER command is used to set the address to the data pointer (the data pointer can be initialized by setting the $\overline{CS}$ to low). When the data pointer is counted up to 31, it then becomes 0 at the next count, and thus it repeats the operation shown below.



It should be noted that, if display data is written sequentially from address 0 in the divide-by-3 time division mode, addresses 30 and 31 will not be written. However, if the data is written in the divide-by-3 time division mode again, data will be written from addresses 30, 31, followed by 0 so that the display data previously written to address 0 will be modified.

2.6 Blinking Data Memory

The blinking data memory stores blinking data used to control display on/off operation (blinking). Blinking operation can be performed in segment units. Each bit in blinking data memory corresponds to a bit in the data memory; if a bit in the blinking data memory is set to 1, the corresponding segment will blink.

The blinking data memory is addressed by the data pointer at the same time the data memory is addressed. Data is written by using the WRITE BLINKING DATA MEMORY command, and bit manipulation can be performed by using the AND BLINKING DATA MEMORY, or OR BLINKING DATA MEMORY command. The BLINKING ON command is used to initiate blinking operation or select the blinking interval (refer to 3.2)

2.7 Display Data Latch

The display data latch stores the data of the 32 × 4-bit segment driver. Each bit of the display data latch corresponds to a bit in the data memory. All contents of the data memory are transferred to the display data latch at the rising edge of $\overline{CS}$, and the contents displayed on the LCD are modified. If blinking is set, the contents of data memory are modified by the contents of blinking data memory and the resulting values are transferred to the display data latch.

The display data written to the display data latch is successively selected by the control function performed by the LCD timing control, and converted to segment drive signal before output.

2.8 LCD Driver

The LCD driver consists of the segment driver and the common driver, and generates the segment drive signal and common drive signal.

The segment driver outputs a segment signal so that the relationship with the common drive signal is select level if the drive data stored in the display data latch is 1. If the drive data stored in the display data latch is 0, the output of the segment driver will be non-select level.

The common drive signal sequentially drives the LCD common poles according to the time divison specificaion.

2.9 LCD Timing Control

The LCD timing control generates the LCD drive timing according to the number of time divisions, the frequency division ratio, and bias method, and supplies it to the LCD driver. In addition, the LCD timing control outputs a $\overline{SYNC}$ signal from the $\overline{SYNC}$ pin in order to synchronize the display timing of each μPD7225 when configured in a multi-chip configuration.

In a multi-chip configuration, the common signal can be used in common or blinking operation can be synchronized by making a wired-OR connection with the $\overline{SYNC}$ pin of each μPD7225.

3. FRAME FREQUENCY AND BLINKING FREQUENCY SETTING

3.1 Frame Frequency Setting

The frame frequency is set according to M1, M0 (number of time-divisions setting), and F1, F0 (frequency division ratio) as indicated in the figure below.

Figure 8. Frame Frequency Setting

		Static		Divide- by-2 time division		Divide- by-3 time division		Divide- by-4 time division	
F1,F0 \ M1, M0		0	1	1	1	1	0	0	0
0	0	$\frac{f_{CL}}{2^7}$		$\frac{f_{CL}}{2^7 \times 2}$		$\frac{f_{CL}}{2^7 \times 3}$		$\frac{f_{CL}}{2^7 \times 4}$	
0	1	$\frac{f_{CL}}{2^8}$		$\frac{f_{CL}}{2^8 \times 2}$		$\frac{f_{CL}}{2^8 \times 3}$		$\frac{f_{CL}}{2^8 \times 4}$	
1	0	$\frac{f_{CL}}{2^9}$		$\frac{f_{CL}}{2^9 \times 2}$		$\frac{f_{CL}}{2^9 \times 3}$		$\frac{f_{CL}}{2^9 \times 4}$	
1	1	$\frac{f_{CL}}{2^{11}}$		$\frac{f_{CL}}{2^{11} \times 2}$		$\frac{f_{CL}}{2^{11} \times 3}$		$\frac{f_{CL}}{2^{11} \times 4}$	

f_{CL} = Clock oscillation frequency

3.2 Blinking Frequency Setting

The blinking frequency can be set in two settings by K0 in the BLINKING ON command.

Figure 9. Blinking Frequency Setting

K0	Blinking frequency
0	$\frac{f_{CL}}{2^{17}}$
1	$\frac{f_{CL}}{2^{16}}$

f_{CL} = Clock oscillation frequency

4. LCD DRIVE POWER SUPPLY PIN VOLTAGE SETTING

The bias method for setting the LCD drive power supply pin allows a different voltage to be supplied to each pin.

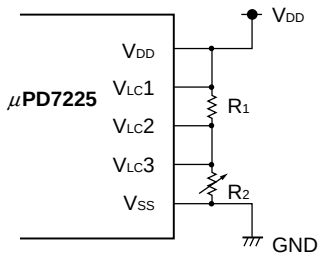
Figure 10. Voltage Setting

	V_{LC1}	V_{LC2}	V_{LC3}
Static	V_{DD}	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$
1/2 bias	$V_{DD} - \frac{1}{2} V_{LCD}$	$V_{DD} - \frac{1}{2} V_{LCD}$	$V_{DD} - V_{LCD}$
1/3 bias	$V_{DD} - \frac{1}{3} V_{LCD}$	$V_{DD} - \frac{1}{3} V_{LCD}$	$V_{DD} - V_{LCD}$

∗ V_{LCD} : LCD voltage

The following shows a circuit example which supplies voltages between VDD and VSS as the LCD drive reference voltage.

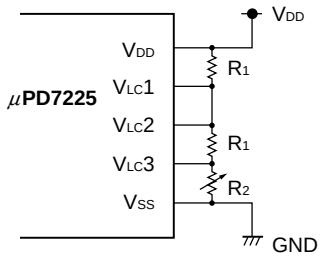
(1) Static



$$R_1 = \frac{V_{LCD}}{V_{DD} - V_{LCD}} \times R_2$$

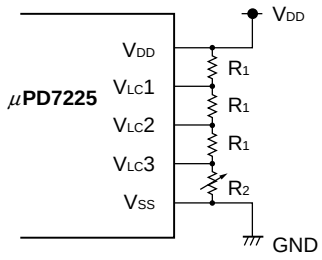
- V_{LCD}: LCD drive voltage
- R_2 is used for contrast adjustment.

(2) Divide-by-2, -3 time division (1/2 bias)



$$R_1 = \frac{V_{LCD}}{2(V_{DD} - V_{LCD})} \times R_2$$

(3) Divide-by-3, -4 time division (1/3 bias)

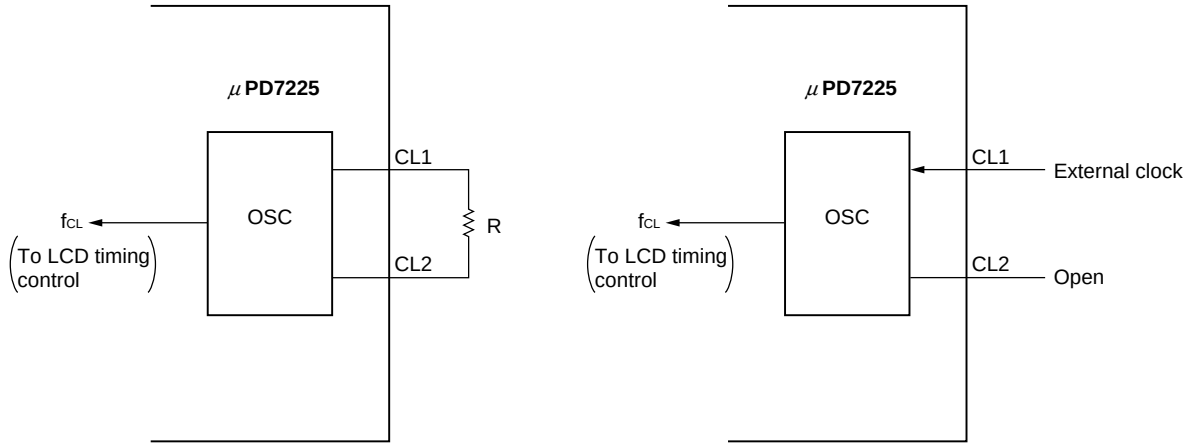


$$R_1 = \frac{V_{LCD}}{3(V_{DD} - V_{LCD})} \times R_2$$

5. CLOCK CIRCUIT

The clock oscillator can be configured by connecting a resistor (R) across the CL1 and CL2 clock pins. When using the external clock, CL1 can be used to input the external clock (CL2: Open).

Figure 11. External Circuit for Clock Oscillation Pins



Remark f_{CL} = Clock oscillation frequency (when using the external clock, this frequency is same as that of the external clock frequency.)

When configuring a multi-chip system using the $\overline{SYNC}$ pin, a clock with the same frequency and same phase must be supplied to the CL1 pin of each μPD7225.

6. RESET FUNCTION

When a low level of 12 clock cycles or more is input to the $\overline{\text{RESET}}$ pin, the μPD7225 will be reset to the following conditions:

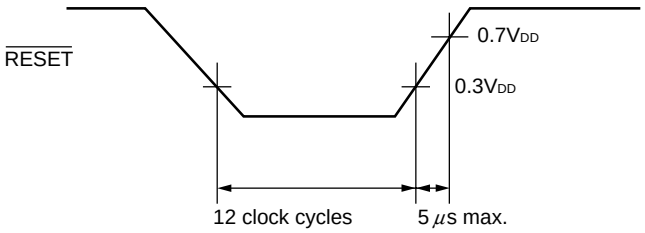
- This condition is the same as when M2 – M0 = 0, F1, F0 = 0 are executed by the MODE SET command.
- Display data transfer from the data memory to the display data latch —– This condition is the same as when the UNSYNCHRONIZED TRANSFER command is executed.
- Command/data register output —– This condition is the same as when the WHITOUT SEGMENT DECODER command is executed.
- LCD display —– This condition is the same as when the DISPLAY OFF or the BRINKING OFF command is executed.

Function when the μPD7225 is reset

- S0-S31 and COM0-COM3 pins output VDD
- Serial data input —– Disabled ($\overline{\text{BUSY}}$ = 0) (However, $\overline{\text{CS}}$ = 0)

When used in a multi-chip system, the reset state must be released (rising edge of $\overline{\text{RESET}}$) within 5 μs.

Figure 12. Reset Signal in Multi-Chip System



7. SERIAL DATA INPUT

Serial data is input to the SI pin with MSB first in synchronization with the serial clock in 8-bits units. When $\overline{CS}$ is set to low, the μPD7225 sets the $\overline{BUSY}$ to low (this initializes the SCK counter and the data pointer to 0) in order to perform internal processing. Therefore, after the μPD7225 completes internal processing, the first bit (MSB) should be input in synchronization with the $\overline{SCK}$ after the $\overline{BUSY}$ signal is set to high. The serial data is transferred to the serial register in bit units at the rising edge of $\overline{SCK}$. Inputting eight serial clocks completes the transfer of all 8 bits of data to the serial register. At the rising edge of the eighth serial clock, the $\overline{BUSY}$ is set to low, and the status of the C/$\overline{D}$ pin is clocked in to specify whether the data is a command or data. Afterwards, the contents of the serial register are clocked into the command/data register.

When successively inputting 2 or more bytes of serial data, $\overline{CS}$ must be set to low until all bytes of data are input. The $\overline{BUSY}$ is set to low each time a byte of data is input. The $\overline{BUSY}$ becomes high when the serial data is clocked in from the serial register to the command/data register, so that the next serial data can be input.

When input of all serial data is complete, the data memory contents can be displayed by setting $\overline{CS}$ to high. $\overline{CS}$ must not be set to high while display data is being transferred (before eight clocks has elapsed.) If it becomes necessary to interrupt serial data transfer when transferring two or more bytes of data due to an interrupt for the CPU interrupt, execute the PAUSE TRANSFER command after checking that the byte has been transferred, then set $\overline{CS}$ to high. In this case, even if $\overline{CS}$ is set to high, the contents of the data memory will not be transferred to the display data latch.

To resume serial data transfer, set $\overline{CS}$ to low in the same way as when initiating a normal transfer. However, in this case, the contents of the data pointer are not cleared so that data write operation starts from the next data memory address when serial data transfer is resumed (C/$\overline{D}$ = 0).

Note In a multi-chip system in which the $\overline{BUSY}$ pins of chips are made a wired-OR connection, avoid setting the $\overline{CS}$ pins of two or more chips simultaneously.

Figure 13. Inputting Byte

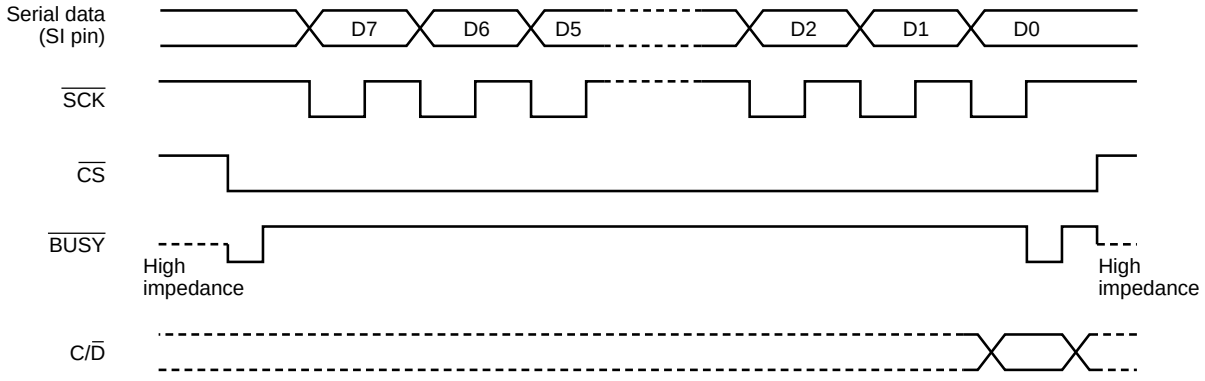
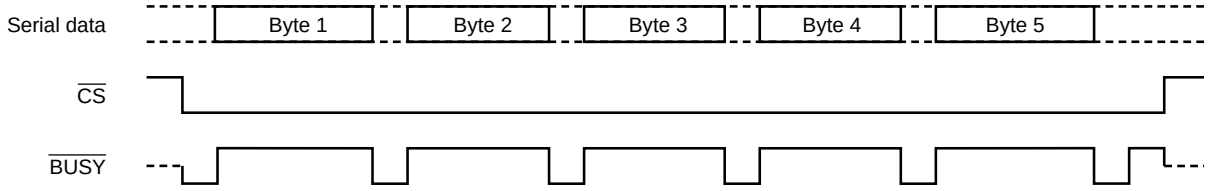


Figure 14. Inputting 5 Bytes Successively



8. COMMAND

8.1 MODE SET

0	1	0	M2	M1	M0	F1	F0

This command sets the number of time divisions for the LCD display static drive or the time-division drive, bias method, and frame frequency.

a. M1 and M0 specify the number of time divisions for static drive or time-division drive.

M1	M0	
0	0	Divide-by-4 time division drive
1	0	Divide-by-3 time division drive
1	1	Divide-by-2 time division drive
0	1	Static drive

b. M2 specifies the bias method.

M2	
0	1/3 bias method
1	1/2 bias method
0/1	Static

c. F1 and F0 specify the frequency division ratio which determines the frame frequency (refer to Figure 8).

F1	F0	Frequency division ratio
0	0	1/27
0	1	1/28
1	0	1/29
1	1	1/211

8.2 SYNCHRONIZED TRANSFER

0	0	1	1	0	0	0	1

This command controls display data modification.

Normally, modification of display data is performed at the rising edge of the $\overline{CS}$ signal (transferring display data from the data memory to the display data latch). However, after this command is executed, display data is modified at the first alternate current drive cycle (Frame frequency x Number of time divisions) after the $\overline{CS}$ signal is set to high.

8.3 UNSYNCHRONIZED TRANSFER

0	0	1	1	0	0	0	0

This command controls display data modification.

After this command is executed, display data is modified at the rising edge of the $\overline{CS}$ pin.

8.4 PAUSE TRANSFER

0	0	1	1	1	0	0	0

This command disables display data modification.

After this command is executed, display data can not be modified at the first rising edge of the $\overline{CS}$ pin; instead, modification is put off until the second rising edge of the $\overline{CS}$ pin. In addition, the data pointer is not cleared at the first rising edge of the $\overline{CS}$ pin (refer to 2.5).

This command is used when it becomes necessary to set the $\overline{CS}$ pin to high due to an interrupt for the CPU in the middle of serial data input operation.

8.5 BLINKING ON

0	0	0	1	1	0	1	K0

This command sets the blinking operation status. The blinking frequency is set by the least significant bit of the command (bit K0).

K0	Blinking frequency (Hz)
0	$f_{CL}/2^{17}$
1	$f_{CL}/2^{16}$

f_{CL}: Clock oscillation frequency

8.6 BLINKING OFF

0	0	0	1	1	0	0	0

This command stops blinking operation.

8.7 DISPLAY ON

0	0	0	1	0	0	0	1

After this command is executed, LCD display operation starts according to the display data contained in the display data latch.

8.8 DISPLAY OFF

0	0	0	1	0	0	0	0

When this command is executed, the relationship of all common drive signals and segment drive signals enters the non-select state. As a result, the display is turned off. Transferring display data from the data memory to the display data latch is not affected by this command execution.

8.9 WITH SEGMENT DECODER

0	0	0	1	0	1	0	1

After this command is executed, input data is sent to the segment decoder, and the decoded code is written to the data memory.

8.10 WITHOUT SEGMENT DECODER

0	0	0	1	0	1	0	0

After this command is executed, input data is written to the data memory without going through the segment decoder.

8.11 LOAD DATA POINTER

1	1	1	D4	D3	D2	D1	D0

This command sets immediate data D4-D0 to the data pointer.

8.12 WRITE DATA MEMORY

1	1	0	1	D3	D2	D1	D0

This command stores immediate data D3-D0 to the data memory addressed by the data pointer, and increments (+1) the contents of the data pointer.

8.13 OR DATA MEMORY

1	0	1	1	D3	D2	D1	D0

This command ORs the contents of the data memory addressed by the data pointer and immediate data D3-D0, and stores the result to the data memory, then increments (+1) the contents of the data pointer.

8.14 AND DATA MEMORY

1	0	0	1	D3	D2	D1	D0

This command ANDs the contents of the data memory addressed by the data pointer and immediate data D3-D0, and stores the result to the data memory, then increments (+1) the contents of the data pointer.

8.15 CLEAR DATA MEMORY

0	0	1	0	0	0	0	0

This command clears the contents of the data memory and the data pointer.

8.16 WRITE BLINKING DATA MEMORY

1	1	0	0	D3	D2	D1	D0

This command stores immediate data D3-D0 to the blinking data memory addressed by the data pointer, and increments (+1) the contents of the data pointer.

8.17 OR BLINKING DATA MEMORY

1	0	1	0	D3	D2	D1	D0

This command ORs the contents of the blinking data memory addressed by the data pointer and immediate data D3-D0, and stores the result to the blinking data memory, then increments (+1) the contents of the data pointer.

8.18 AND BLINKING DATA MEMORY

1	0	0	0	D3	D2	D1	D0

This command ANDs the contents of the blinking data memory addressed by the data pointer and immediate data D3-D0, and stores the result to the blinking data memory, then increments (+1) the contents of the data pointer.

8.19 CLEAR BLINKING DATA MEMORY

0	0	0	0	0	0	0	0

This command clears the contents of the blinking data memory and the data pointer.

9. DISPLAY OUTPUT

The following describes the serial data organization, display data organization in the data memory, segment drive signal, and common drive signal when the display is active in the static and divide-by-2, -3, -4 time division modes.

9.1 Static

When displaying just the digit “6” in the static mode:

a. Serial data organization: 0D, 07

b. Display data organization in the data memory

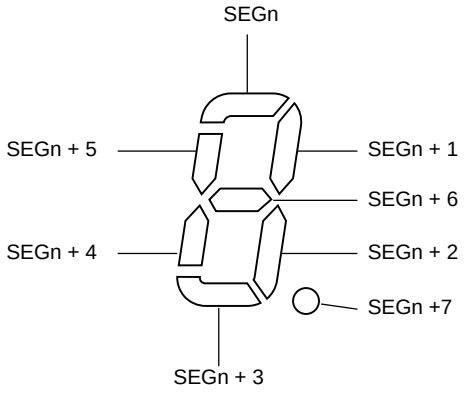
		Address							
		n + 7	n + 6	n + 5	n + 4	n +3	n + 2	n + 1	n
Bit	Contents of bit 0	0	1	1	1	1	1	0	1

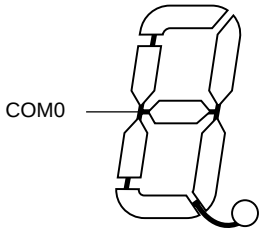
c. Power supply (static)

$V_{LC0} = V_{LC1} = V_{DD}$

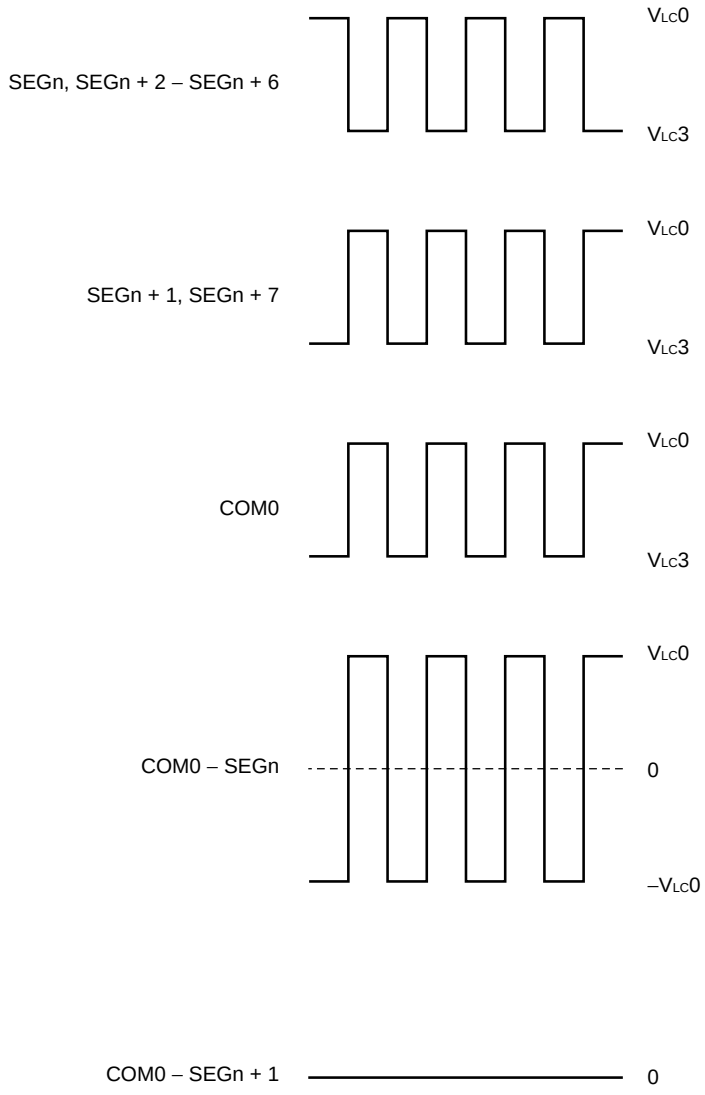
$V_{LC2} = V_{LC3} = V_{DD} – V_{LCD}$

d. Relationship between common and segment





e. Segment and common drive signals



9.2 Divide-by-2 Time Division

When displaying just the digit “6” in the divide-by-2 time division mode:

a. Serial data organization: F5

b. Display data organization in the data memory

		Address			
		n +3	n + 2	n + 1	n
Bit	Contents of bit 0	1	1	1	1
	Contents of bit 1	1	1	0	0

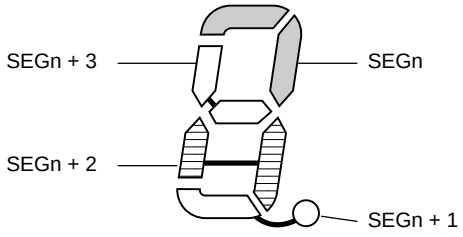
c. Power supply (1/2 bias)

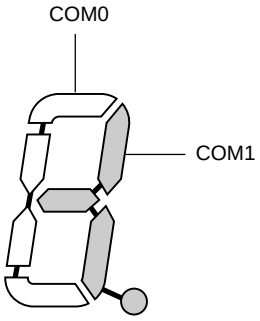
$V_{LC0} = V_{DD}$

$V_{LC1} = V_{LC2} = V_{DD} - 1/2\ V_{LCD}$

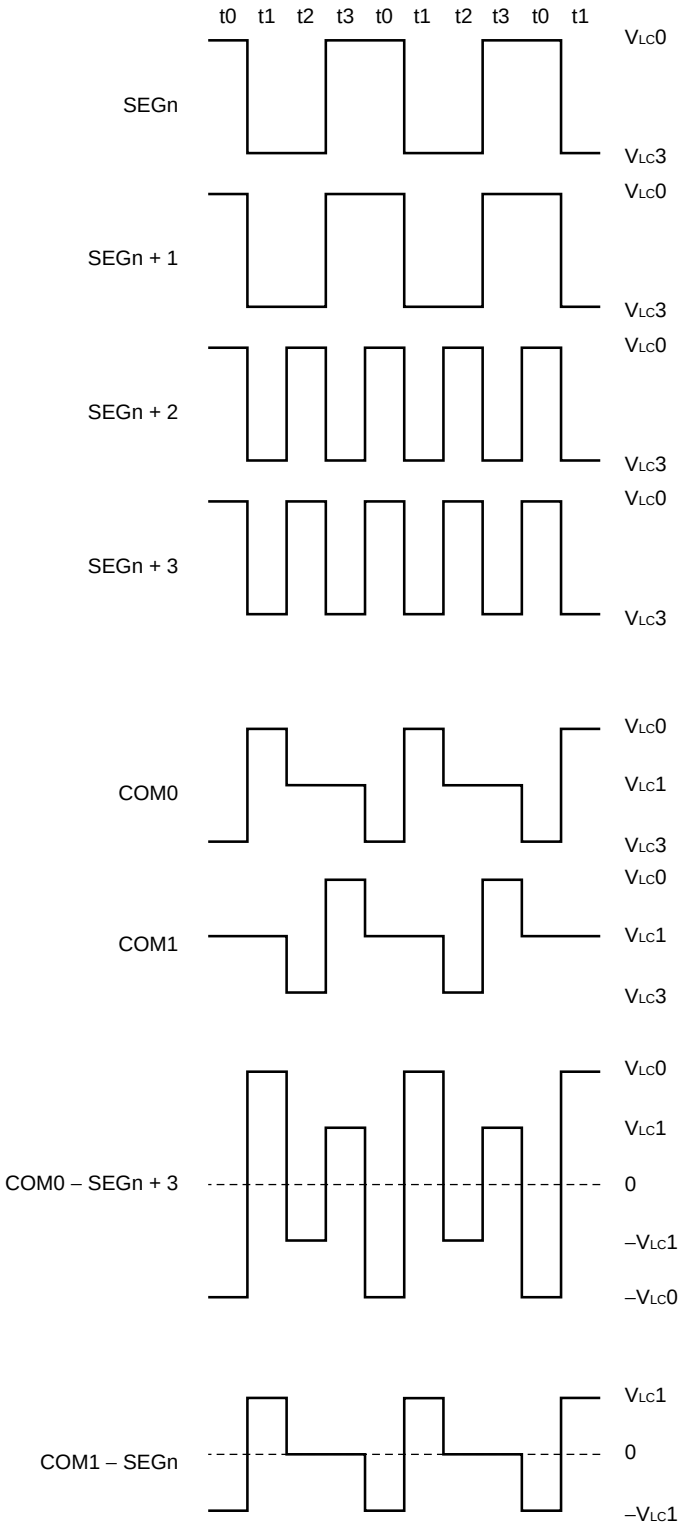
$V_{LC3} = V_{DD} - V_{LCD}$

d. Relationship between common and segment





e. Segment and common drive signals



9.3 Divide-by-3 Time Division

When displaying the digit “6.” in the divide-by-3 time division mode:

a. Serial data organization
   - Without segment decoder: FE
   - With segment decoder : 06

   (However, the floating point is set to “1” by command.)

b. Display data organization in the data memory

		Address		
		n + 2	n + 1	n
Bit	Contents of bit 0	1	1	0
	Contents of bit 1	1	1	1
	Contents of bit 2	0	1	1

c. Power supply (1/3 bias)

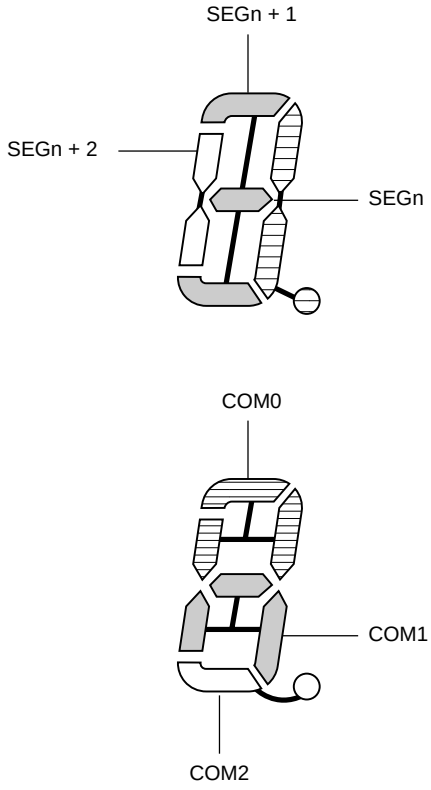
$V_{LC0} = V_{DD}$

$V_{LC1} = V_{DD} - 1/3\ V_{LCD}$

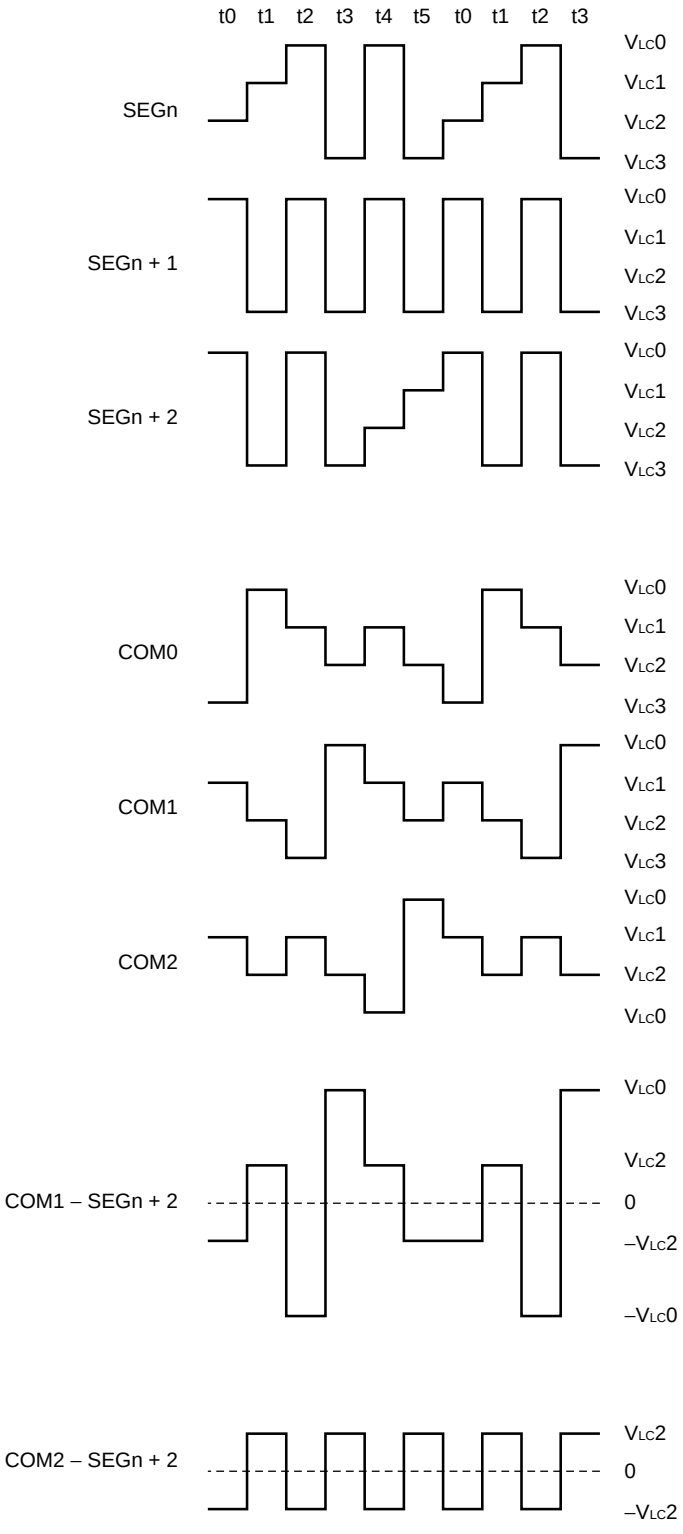
$V_{LC2} = V_{DD} - 2/3\ V_{LCD}$

$V_{LC3} = V_{DD} - V_{LCD}$

d. Relationship between common and segment



e. Segment and common drive signals



9.4 Divide-by-4 Time Division

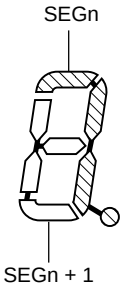
When displaying the digit “6.” in the divide-by-4 time division mode:

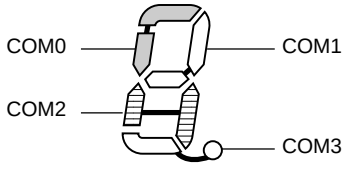
a. Serial data organization
   - Without segment decoder: FD
   - With segment decoder : 06
     (However, the floating point is set to “1” by command.)

		Address	
		n + 1	n
Bit	Contents of bit 0	1	1
	Contents of bit 1	1	0
	Contents of bit 2	1	1
	Contents of bit 3	1	1

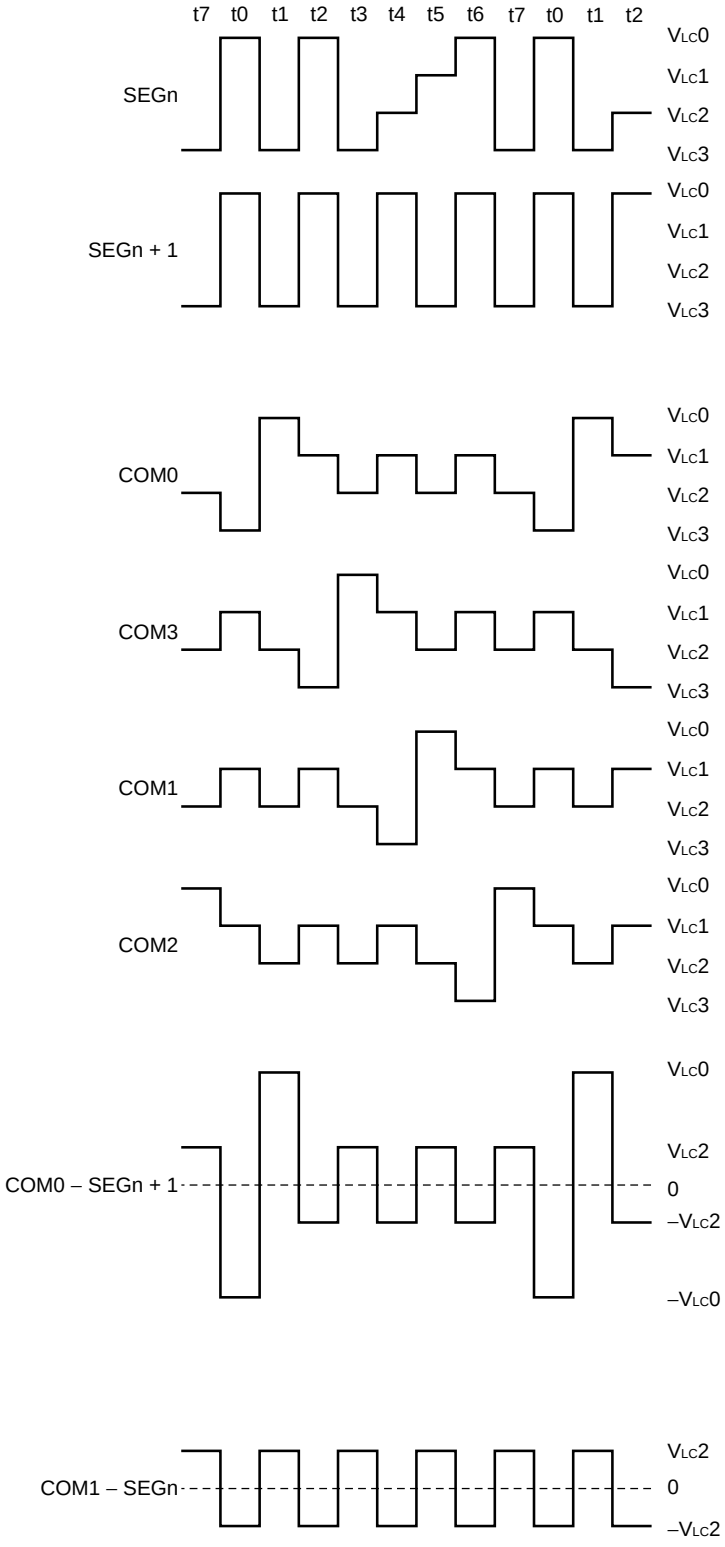
b. Power supply (1/3 bias)
   $V_{LC0} = V_{DD}$
   $V_{LC1} = V_{DD} - 1/3\ V_{LCD}$
   $V_{LC2} = V_{DD} - 2/3\ V_{LCD}$
   $V_{LC3} = V_{DD} - V_{LCD}$

c. Relationship between common and segment





d. Segment and common drive signals



10. ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating (T_a = 25 °C)

Item	Symbol	Condition	Rating	Units
Power supply voltage	V_{DD}		−0.3 to +7.0	V
Input voltage	V_I		−0.3 to V_{DD} +0.3	V
Output voltage	V_O		−0.3 to V_{DD} +0.3	V
Operating temperature	T_{opt}		−10 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

DC Characteristics (T_a = −10 to +70 °C, V_{DD} = 5 V ± 10%)

Item	Symbol	Condition	Specification			Units
			MIN.	TYP.	MAX.	
High level input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Low level input voltage	V_{IL}		0		0.3 V_{DD}	V
High level output voltage	V_{OH}	$\overline{SYNC}$, $\overline{BUSY}$, I_{OH} = −10 μA	V_{DD} − 0.5			V
Low level output voltage	V_{OL1}	$\overline{BUSY}$, I_{OL} = 100 μA			0.5	V
	V_{OL2}	$\overline{SYNC}$, I_{OL} = 900 μA			1.0	V
Output short-circuit current	I_{OS}	$\overline{SYNC}$, V_O = 1 V			−300	μA
High level input leakage current	I_{LIH}	$V_I = V_{DD}$			2	μA
Low level input leakage current	I_{LIL}	V_I = 0 V			−2	μA
High level output leakage current	I_{LOH}	$V_O = V_{DD}$			2	μA
Low level output leakage current	I_{LOL}	V_O = 0 V			−2	μA
Common output impedance	R_{COM}	COM0 to COM3*[1], $V_{DD} \geq V_{LCD}$		5	7	kΩ
Segment output impedance	R_{SEG}	S0 to S31*[1], $V_{DD} \geq V_{LCD}$		7	14	kΩ
Power supply voltage	I_{DD}	CL1 external clock, f_C = 200 kHz*		100	250	μA

∗ Abnormal current will flow if the external clock supply is removed.

Remark ∗1. Applies to Static, 1/2 bias, 1/3 bias

AC Characteristics (T_a = –10 to +70 °C, V_{DD} = 5 V ± 10%)

Item	Symbol	Condition	Specification			Units
			MIN.	TYP.	MAX.	
Operating frequency	f_C		50		200	kHz
Oscillation frequency	f_{OSC}	R = 180 kΩ ± 5%	85	130	175	kHz
High level clock pulse width	t_{WHC}	CL1, external clock	2		16	μs
Low level clock pulse width	t_{WLC}	CL1, external clock	2		16	μs
$\overline{SCK}$ frequency	t_{CYK}		900			ns
High level $\overline{SCK}$ pulse width	t_{WHK}		400			ns
Low level $\overline{SCK}$ pulse width	t_{WLK}		400			ns
$\overline{BUSY}$ ↑→ $\overline{SCK}$ ↓ hold time	t_{HBK}		0			ns
SI set time (against $\overline{SCK}$ ↑)	t_{SIK}		100			ns
SI hold time (against $\overline{SCK}$ ↑)	t_{HKI}		200			ns
8th pulse of $\overline{SCK}$ ↑→ $\overline{BUSY}$ ↓ delay time	t_{DKB}	C_L = 50 pF			3	μs
$\overline{CS}$ ↓→ $\overline{BUSY}$ ↓ delay time	t_{DCSB}	C_L = 50 pF			1.5	μs
$\overline{BUSY}$ low level time	t_{WLB}	$t_{WHCS} \geq 48/f_C$ *2 C_L = 50 pF	4		44 (57)*3	$1/f_C$
C/$\overline{D}$ set time (against 8th pulse of SCK ↑)	t_{SDK}		9			μs
C/$\overline{D}$ hold time (against 8th pulse of SCK ↑)	t_{HKD}		1			μs

Remark ∗**2**. UNSYNCHRONIZED TRANSFER MODE
For SYNCHRONIZED TRANSFER MODE,
$t_{WHCS} \geq$ (48/f_C + AC driver frequency)

∗**3**. BLINKING ON

Item	Symbol	Condition	Specification			Units
			MIN.	TYP.	MAX.	
$\overline{CS}$ hold time (against 8th pulse of SCK ↑)	t_{HKCS}		1			μs
High level $\overline{CS}$ pulse width	t_{WHCS}		**∗4**			μs
Low level $\overline{CS}$ pulse width	t_{WLCS}		**∗4**			μs
$\overline{SYNC}$ load capacitance	C_{LSY}	t_{CYC} = 5 μs			50	pF

Remark ∗**4**. 8/f_C

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Item	Symbol	Condition		Rating			Units
				MIN.	TYP.	MAX.	
Input capacitance	C_{IN}		f = 1 MHz pins other than those used for measurement are 0 V.			10	pF
Output capacitance	C_{OUT1}	Except $\overline{BUSY}$				20	pF
Output capacitance	C_{OUT2}	$\overline{BUSY}$				15	pF
Input/output capacitance	C_{IO}	$\overline{SYNC}$				15	pF
Clock capacitance	C_C	CL1				30	pF

DC Characteristics (T_a = 0 to +70 °C, V_{DD} = 2.7 to 5.5 V)

Item	Symbol	Condition	Specification			Units
			MIN.	TYP.	MAX.	
High level input voltage	V_{IH1}	Except $\overline{SCK}$	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{SCK}$	0.8 V_{DD}		V_{DD}	V
Low level input voltage	V_{IL1}	Except $\overline{SCK}$	0		0.3 V_{DD}	V
	V_{IL2}	$\overline{SCK}$	0		0.2 V_{DD}	V
High level output voltage	V_{OH}	$\overline{SYNC}$, $\overline{BUSY}$, I_{OH} = −7 μA	V_{DD} − 0.75			V
Low level output voltage	V_{OL1}	$\overline{BUSY}$, I_{OL} = 100 μA			0.5	V
	V_{OL2}	$\overline{SYNC}$, I_{OL} = 400 μA			0.5	V
Output short-circuit current	I_{OS}	$\overline{SYNC}$, V_O = 0.5 V			−200	μA
High level input leakage current	I_{LIH}	$V_I = V_{DD}$			2	μA
Low level input leakage current	I_{LIL}	V_I = 0 V			−2	μA
High level output leakage current	I_{LOH}	$V_O = V_{DD}$			2	μA
Low level output leakage current	I_{LOL}	V_O = 0 V			−2	μA
Common output impedance	R_{COM}	COM0 to COM3*[1], $V_{DD} \geq V_{LCD}$		6		kΩ
Segment output impedance	R_{SEG}	S0 to S31*[1], $V_{DD} \geq V_{LCD}$		12		kΩ
Power supply voltage	I_{DD}	CL external clock, V_{DD} = 3 V ± 10%, f_C = 140 kHz*		30	100	μA

∗ Abnormal current will flow if the external clock supply is removed.

Remark ∗**1**. Applies to Static and 1/3 bias

AC Characteristics (T_a = 0 to +70 °C, V_{DD} = 2.7 V to 5.5 V)

Item	Symbol	Condition	Specification			Units
			MIN.	TYP.	MAX.	
Operating frequency	f_C		50		140	kHz
Oscillation frequency	f_{OSC}	R = 180 kΩ ± 5%, V_{DD} = 3 V ± 10 %	50	100	140	kHz
High level clock pulse width	t_{WHC}	CL1, external clock	3		16	μs
Low level clock pulse width	t_{WLC}	CL1, external clock	3		16	μs
$\overline{SCK}$ frequency	t_{CYK}		4			μs
High level $\overline{SCK}$ pulse width	t_{WHK}		1.8			μs
Low level $\overline{SCK}$ pulse width	t_{WLK}		1.8			μs
$\overline{BUSY}$ ↑→ $\overline{SCK}$ hold time	t_{HBK}		0			ns
SI set time (against $\overline{SCK}$ ↑)	t_{SIK}		1			μs
SI hold time (against $\overline{SCK}$ ↑)	t_{HKI}		1			μs
8th pulse of $\overline{SCK}$ ↑→ $\overline{BUSY}$ ↓ delay time	t_{DKB}	C_L = 50 pF			5	μs
$\overline{CS}$ ↓→ $\overline{BUSY}$ ↓ delay time	t_{DCSB}	C_L = 50 pF			5	μs
BUSY low level time	t_{WLB}	$t_{WHCS} \geq 48/f_C$ *2 C_L = 50 pF	4		44 (57)*3	$1/f_C$
C/$\overline{D}$ set time (against 8th pulse of SCK ↑)	t_{SDK}		18			μs
C/$\overline{D}$ hold time (against 8th pulse of SCK ↑)	t_{HKD}		1			μs

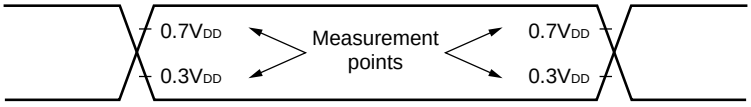
Remark ∗**2**. UNSYNCHRONIZED TRANSFER MODE
For SYNCHRONIZED TRANSFER MODE,
$t_{WHCS} \geq (48/f_C$ + AC driver frequency)

∗**3**. BLINKING ON

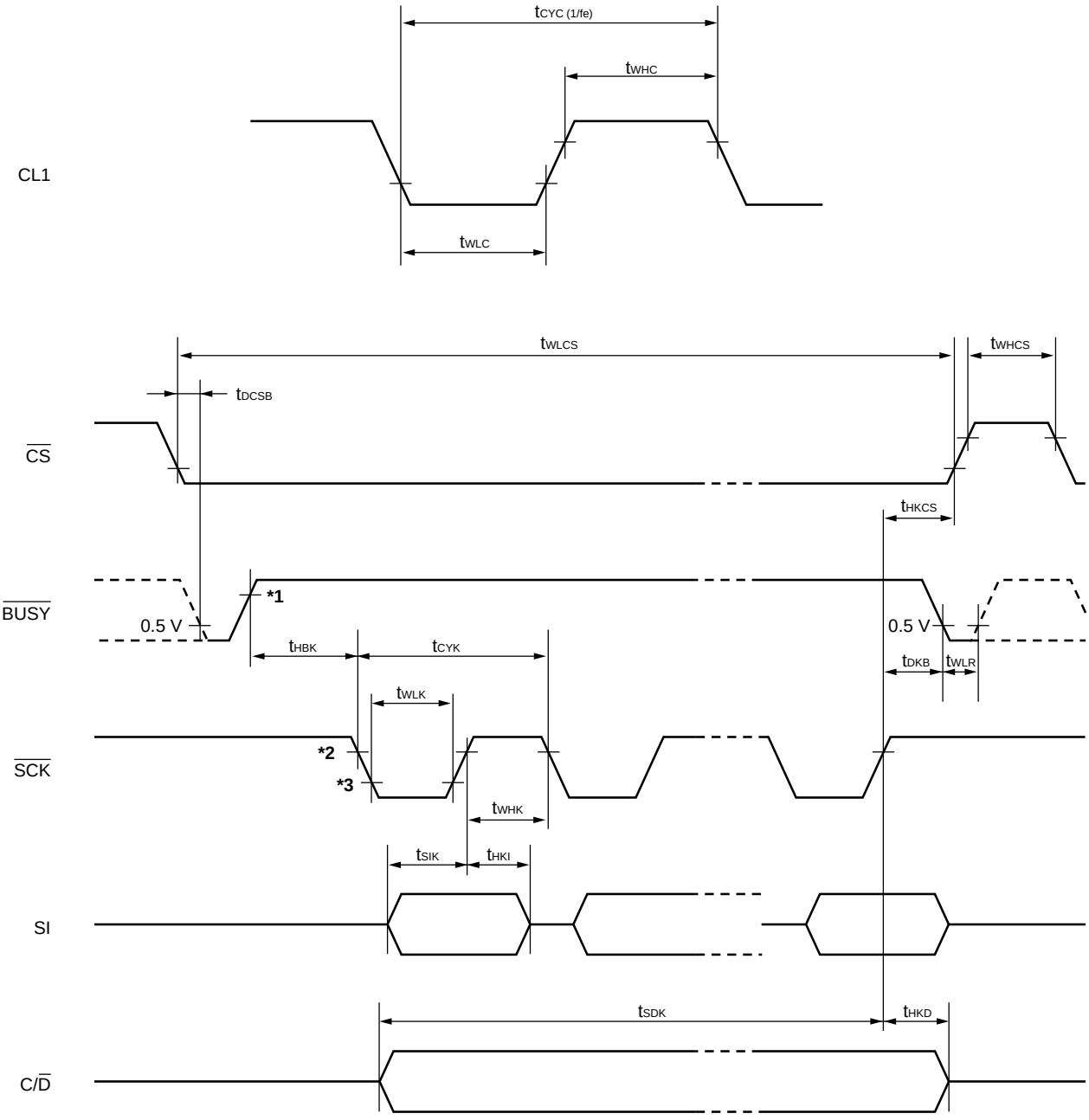
Item	Symbol	Condition	Specification			Units
			MIN.	TYP.	MAX.	
$\overline{CS}$ hold time (against 8th pulse of SCK ↑)	t_{HKCS}		1			μs
High level $\overline{CS}$ pulse width	t_{WHCS}		∗**4**			μs
Low level $\overline{CS}$ pulse width	t_{WLCS}		∗**4**			μs
$\overline{SYNC}$ load capacitance	C_{LSY}	t_{CYC} = 7.1 μs			50	pF

Remark ∗**4**. $8/f_C$

AC Timing Measurement Voltage



Timing Wave-Form



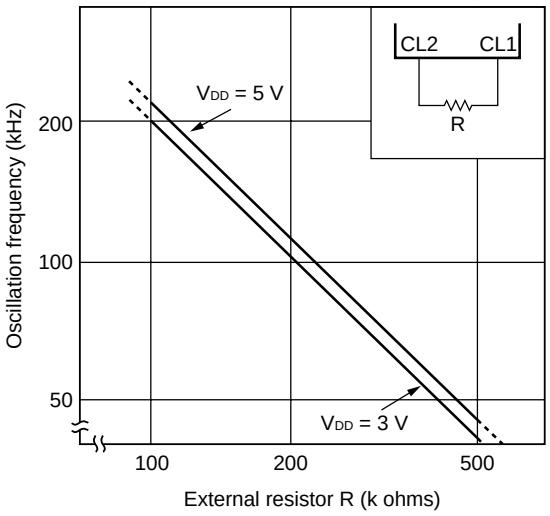
∗**1.** V_{DD} – 0.5 V when V_{DD} = 5 V ± 10 %, V_{DD} – 0.75 V when V_{DD} = 2.7 to 5.5 V

∗**2.** 0.8 V when V_{DD} = 2.7 V to 5.5 V

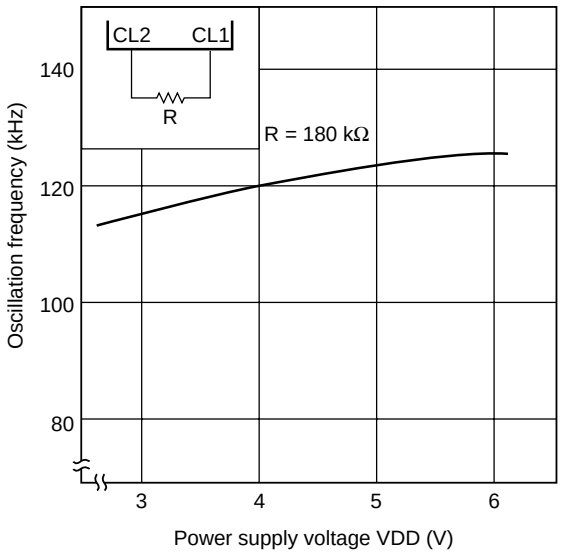
∗**3.** 0.2 V when V_{DD} = 2.7 V to 5.5 V

Typical Characteristic Curve (T_a = 25 °C)

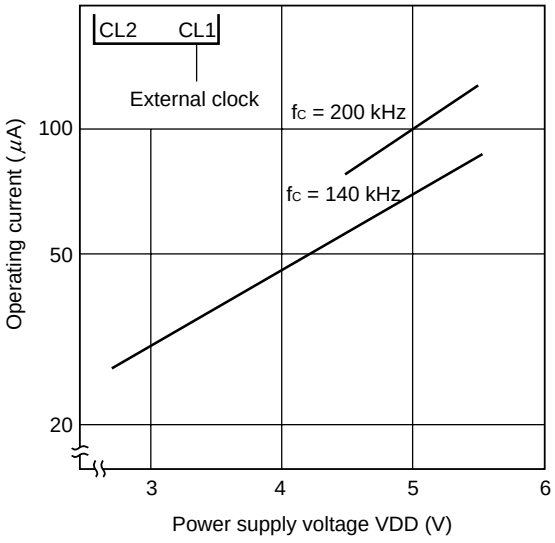
External resistor and oscillation frequency



Power supply voltage and oscillation frequency

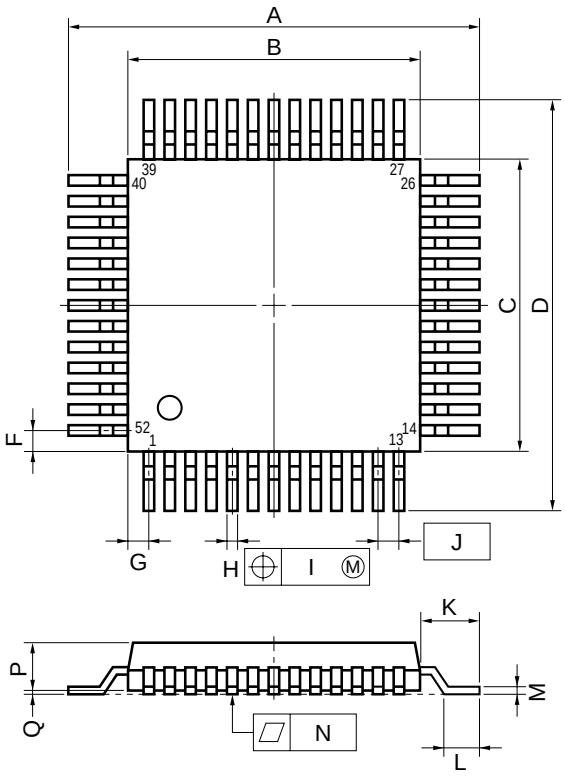


Power supply voltage and operating current

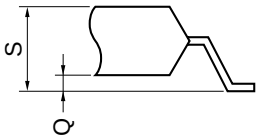


11. DIMENSIONS

52 PIN PLASTIC QFP (□14)



detail of lead end



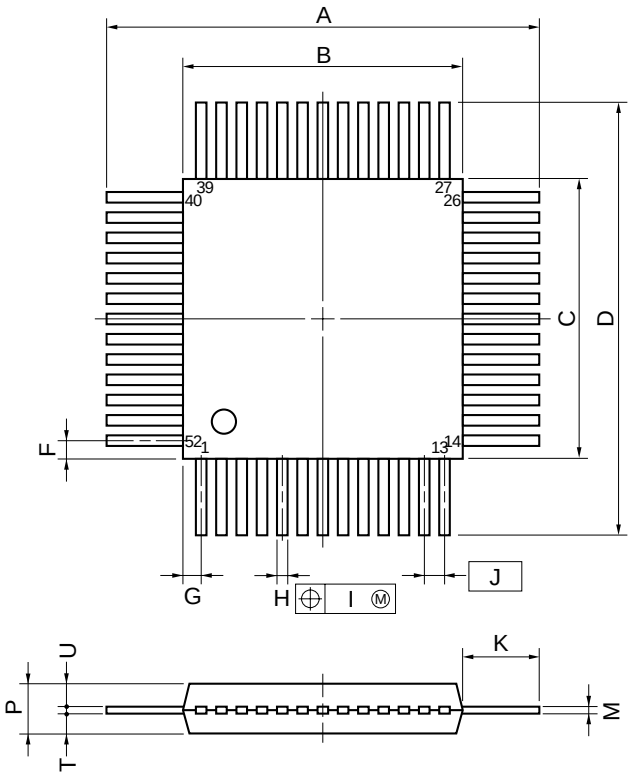
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.0±0.4	0.827±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	21.0±0.4	0.827±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	3.5±0.2	$0.138^{+0.008}_{-0.009}$
L	2.2±0.2	$0.087^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	$2.6^{+0.2}_{-0.1}$	$0.102^{+0.009}_{-0.004}$
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

P52G-100-00-2

52PIN PLASTIC QFP (STRAIGHT) (□14)



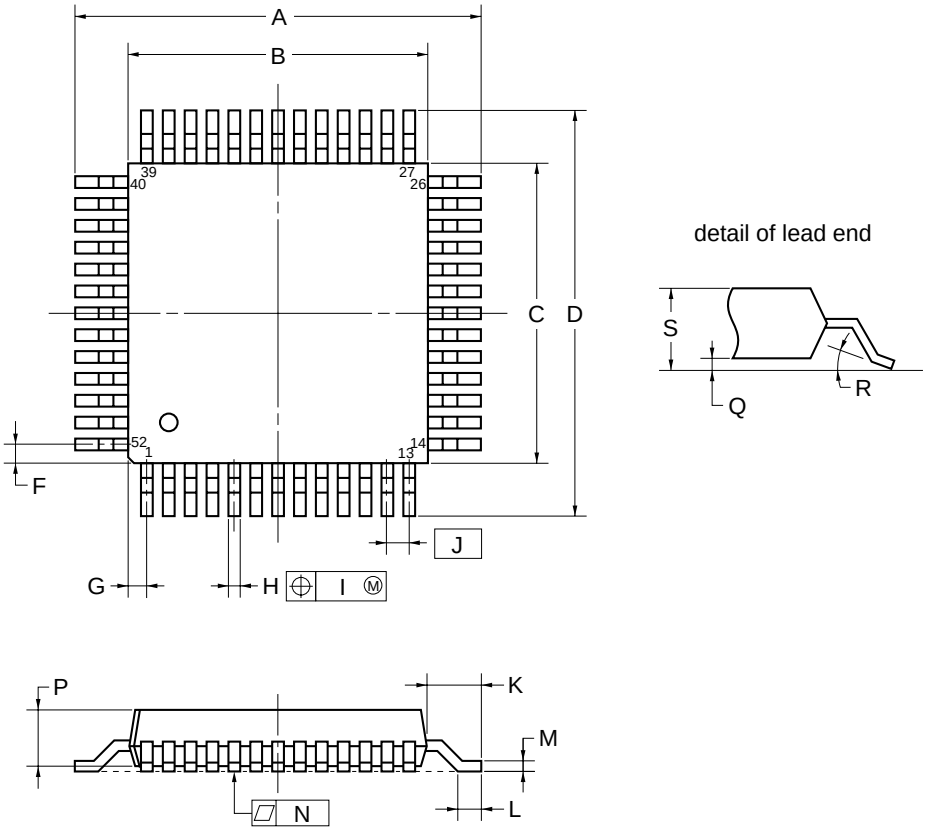
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.4	0.866±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	22.0±0.4	0.866±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	4.0±0.2	$0.157^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
P	$2.6^{+0.2}_{-0.1}$	$0.102^{+0.009}_{-0.004}$
T	1.0	0.039
U	1.45	0.057

P52G-100-01-2

56 PIN PLASTIC QFP (10×10)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.4	0.520±0.016
B	10.0±0.2	0.394±0.008
C	10.0±0.2	0.394±0.008
D	13.2±0.4	0.520±0.016
F	0.75	0.030
G	0.75	0.030
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S56GB-65-3B7-3

12. RECOMMENDED SOLDERING CONDITIONS

When mounting the μPD7225 by soldering, soldering should be performed under the following recommended conditions.

Should other than recommended conditions be used, consult with our sales personnel.

Table 1. Recommended Soldering Conditions

Product	Package	Recommended conditions reference code
μPD7225 G00	52-pin plastic QFP	Pin partial heating
μPD7225 G01		
μPD7225 GB-3B7	56-pin plastic QFP	IR30-00
		VP15-00

Table 2. Soldering Conditions

Recommended conditions reference code	Soldering method	Soldering conditions
IR30-00	Infrared reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (210 °C min.), Number of soldering operations: 1
VP15-00	VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of soldering operations: 1
Pin partial heating	Pin partial heating	Pin temperature: 300 °C max., Time: 10 seconds max.

Note Do not use different soldering methods together (however, the pin partial heating can be used with the other soldering methods).

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Anti-radioactive design is not implemented in this product.

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