Design and Simulation of a Low Power Bluetooth Transceiver

A Technical Report

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Hemant Savla

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Under the guidance of

Prof. Charlie Chung-Ping Chen

Department of Electrical and Computer Engineering
University of Wisconsin-Madison

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Abstract

This technical report demonstrates a fully integrated 2.4 GHz Bluetooth Transceiver in 0.18μm CMOS Technology. A Low IF (3Mhz) receiver architecture and direct modulation architecture is chosen for the transmitter to minimize the chip area and power consumption. To reduce the power consumption, the whole transceiver is designed to operate at 1.5V.

The designed transceiver integrates all building blocks on-chip, including a RF switch, low-noise amplifier (LNA) with an input match network, an image rejection Mixer (IRM), gm-C Bandpass filter, Limiter, RSSI, a DLL based Demodulator, Clock and Data recovery (CDR) circuit, fractional-N synthesizer, ΣΔ D/A and a Power Amplifier.

The proposed transceiver has been designed and simulated with TSMC 0.18μm Mixed Mode CMOS technology. The receiver achieves a sensitivity of –80 dBm at 0.1% BER. The direct conversion transmitter delivers GFSK modulated waveform at a nominal output power of 4 dBm. This research confirms the integration of whole transceiver in standard CMOS process, which makes it possible to integrate both Analog transceiver and digital baseband parts on single wafer. This would lower the overall system cost.

Academic Advisor: Chen, Charlie Chung-Ping

Title: Assistant Professor, Department of Electrical and Computer Engineering

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1. Introduction

Bluetooth is a short-range wireless communication standard designed with an intention of replacing cables connecting portable and desktop devices and build low cost networks for such devices. Bluetooth operates in the ISM band (2.4 GHz –2.48 GHz) with GFSK (Gaussian Frequency Shift Key) modulation (BT = 0.5, m = 0.28-0.35)[1]. The operating band of 83.5 MHz is divided into 1 MHz spaced channels, each signaling data at 1 MSPS. The ISM band is occupied by a plethora of RF emitters. To cope with such a hostile environment, Bluetooth uses frequency hopping, power control and short data packets. Although the Bluetooth standards are very well defined but for the mass acceptance of it a SoC IC having low cost and consuming low power is necessary.

Until recently, radio frequency integrated circuits (RFIC's) were implemented in GaAs and SiGe technologies because of their relatively high unity gain cutoff frequency f_T [2]. But due to recent advances in CMOS technology, the minimum feature size of CMOS device is decreasing and as a result the f_T of the transistors continues to improve and has reached to a point where f_T of CMOS is comparable to those in GaAs and SiGe processes. With deep sub-micron CMOS device, f_T exceeding 30Ghz and minimum noise figure less than 0.5 dB could be achieved. Due to these good RF characteristics and other advantages like low cost and possibility of integrating RF, IF and Baseband blocks of transceiver on single substrate, CMOS is becoming most preferred technology for new low cost wireless communications applications like Wireless LAN, Bluetooth, etc [3]-[7].

This report demonstrates a monolithic CMOS wireless transceiver for Bluetooth System with an extremely high level of integration, with any off-chip components. The transceiver integrates all building blocks on-chip, including a RF switch, low-noise amplifier (LNA) with an input match network, an image rejection Mixer (IRM), gm-C filter, Limiter, RSSI, a DLL based Demodulator, Clock and Data recovery (CDR) circuit, fractional-N synthesizer, $\Sigma\Delta$ D/A and a Power Amplifier. The entire design is based on TSMC CMOS 0.18um Mixed Mode technology, which makes it possible to integrate both Analog transceiver and digital baseband parts on single wafer. This would lower the overall system cost.

A Low IF (3MHz) architecture is chosen to minimize the area and power consumption [8]. All the baseband parts are kept fully differential to minimize the substrate coupling. An Open modulation with

sigma-delta modulated fractional-N frequency synthesizer based transmitter was chosen to reduce the power consumption and reduce the area. One of the most effective way of reducing the power consumption is to lower the supply voltage. As of now, a number of radio transceivers working at supply voltages between 3.5V and 1.8V have been reported. [2],[9]-[7]. The radio design presented in this report has been tested to be able to work at 1.5V.

The rest of the report is organized as follows. In chapter 2 the pros and cons of various transceiver architectures are briefly described, then the architecture of the proposed transceiver is presented. The system specification for the receiver and each block of the receiver are also derived and discussed in this chapter. Then from chapter 3 to 10 the design of each components of transceiver that is LNA (Low Noise Amplifer), IRM (Image Rejection Mixer), Bandpass Filter, GFSK Modulator and Demodulator, CDR (Clock and Data Recovery), ΣΔ D/A and Frequency Synthesizer are described in detail. Finally in chapter 11, the conclusion and possible improvements of the transceiver are presented.

2. Transceiver Architecture

System level design of the transceiver is discussed in this chapter. First it starts with the discussion of the Bluetooth specification. Then Specification of the receiver and of each building block is derived. The simulation results of the system level transceiver designed are then discussed.

2.1 Bluetooth Radio layer specification

Bluetooth devices use 2.4-2.483Ghz unlicensed ISM band [1]. It is divided into 78 channels with a channel spacing of 1 MHz.

$$f = 2402 + k \text{ MHz}; k = 0,\ldots..,78$$

In order to comply with out-of-band regulation a lower guard band of 2 Mhz and Upper guard band of 3.5 Mhz is kept. A Frequency hoping spread spectrum technique is used to combat the interferences and fading.

A GFSK (Gaussian Frequency Shift Keying) with a bandwidth-bit time period BT=0.5 and modulation index between 0.28 and 0.35 is used. A binary one is represented by a positive frequency deviation, while binary zero is represented by a negative frequency deviation. A symbol rate of 1 Ms/s is used. For fully duplex transmission, a Time Division duplex (TDD) scheme is used.

Receiver's performance is often measured in terms of its sensitivity [16]. Although the performance of a wireless communication system is often specified in terms of bit error rate (BER) which is very impractical for the receiver front-end design. As a receiver front end can only be evaluated by adding unwanted signals, such as noise, image signals and intermodulation signals, to the wanted signal, the performance can therefore be translated into the specification of SNR (Signal to Noise Ratio). The sensitivity of a receiver is defined as minimum signal power at the input of the receiver which give the required SNR at the output of the receiver. According to the Bluetooth specification a receiver needs to have a sensitivity of –70dBm or bellow.

The interference performance on Co-channel and adjacent 1 MHz and 2 MHz shall be measured with the wanted signal 10 dB over the reference sensitivity level. Signal to interference ratio for various Adjacent and co-channel interference is given in table 2.1 bellow.

Table 2-1 Adjacent and Co-channel Interference Specification

Frequency of Interference	Ratio
Co-Channel interference, $C/I_{co\text{-}channel}$	11 dB
Adjacent (1Mhz) interference, C/I_{1MHz}	0 dB
Adjacent (2Mhz) interference, C/I_{2MHz}	-30 dB
Adjacent (≥3MHz) interference, $CI_{\geq 3MHz}$	-40 dB
Image frequency Interference, C/I_{image}	-9 dB
Adjacent (1 MHz) interference to in-band image frequency, $C/I_{image\pm 1\ MHz}$	-20 dB

Receiver should also be able to block various out of band interference signals located in various bands as given in table 2.2 bellow

Table 2-2 Out of Band Interference Specification

Interfering Signal Frequency	Interfering Signal Power Level
30Mhz- 2000 Mhz	-10 dBm
2000-2399 Mhz	-27 dBm
2484-3000 Mhz	-27 dBm
3000Mhz – 12.75 Ghz	-10 dBm

Depending upon the amount of power transmitted by the power amplifier, transmitters are classified into 3 power class as shown in table 2.3. Power control in not mandatory of power class 2 and 3 but is recommended to save power consumption.

Table 2-3 Transmitter Power Classes

Power class	Max Output Power	Nominal Output Power	Minimum Output Power	Power Control
1	100 mW (20 dBm)	N/A	1mW (0dBm)	Required
2	2.5 mW (4 dBm)	1 mW (0 dBm)	0.25 mW (-6 dBm)	Optional
3	1mW (0 dBm)	N/A	N/A	Optional

2.2 Survey of Transceiver Architecture

2.2.1 Receiver Architecture

Various different architectures can be used to implement Bluetooth receiver [8], eg high IF, low IF and zero IF. All these use only a single conversion with a channel select filtering at only one frequency, which is enabled by the relaxed interference requirements in the Bluetooth specifications.

High IF does a single conversion to an IF that is much greater than the channel bandwidth. Even though they could achieve high image rejection and use smaller passive components, they are not preferred for single chip Bluetooth system as they need a RF and high Q IF channel selection filters, which are tough to fabricate.

Low IF systems down converts to an IF that is greater than the channel bandwidth, usually in 5-10 Mhz range. Here percent bandwidth of the channel select filter is 10-20 percent, which allows the use of lower Q components to create the channel select filter. But this architecture would need an image rejection mixer.

Zero IF system doesn't have the problem of image signal, but it suffers from the problem of DC offset and flicker noise. Block diagrams for all these receiver architectures are shown in figure 2.1

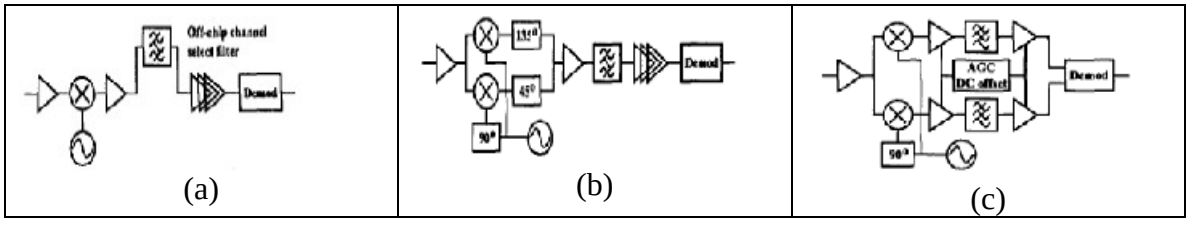


Figure 2-1 Different Receiver Architecture

2.2.2 Transmitter Architecture

The transmitter architecture can be classified into two basic types, transmitter with mixers and transmitter without mixer (also called direct modulation). The former type includes direct-conversion transmitters and two-step transmitters. The later type uses a frequency synthesizer to directly modulate the baseband signal to the RF frequency.

In direct modulation, the baseband digital signals are first filtered by a Gaussian filter, which reduces the side lobe of the output spectrum. The filtered signal is then fed to the VCO, which generates the gfsk modulations. The output signals from the VCO are then amplified using Power amplifier before they are transmitted on antenna. Here system's area and power consumption is reduced as no filters and mixers are being used.

2.3 Architecture of proposed Transceiver

A low IF topology with an intermediate frequency of 3 MHz was chosen over traditional super-heterodyne architecture as it achieves a good SNR (signal to noise ratio) at IF without severe 1/f noise and DC offset problems, it also helps to reduce the power consumption [2]. A top-level block Diagram of the transceiver is shown in figure 2.2.

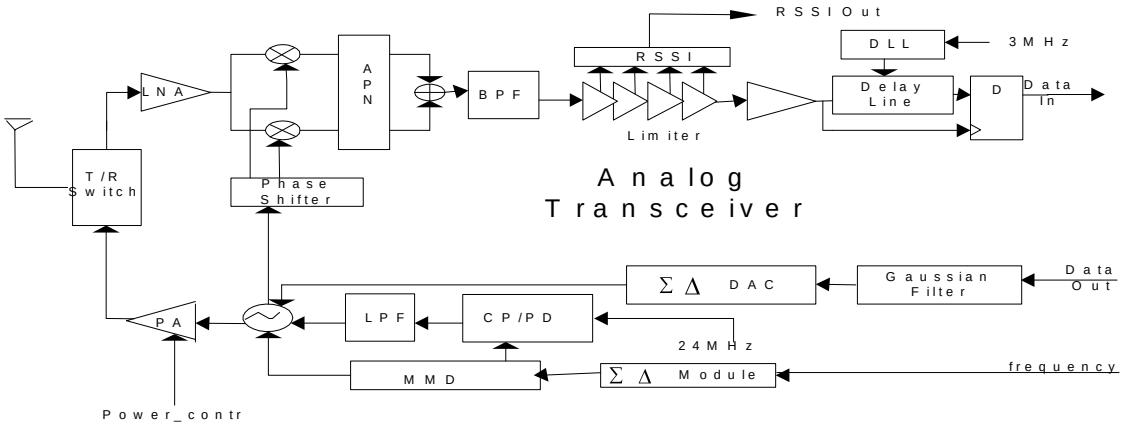


Figure 2.2 Block Diagram of Analog Transceiver

The receiver chain consists of a temperature compensated LNA and IR Mixer (Image Rejection). Image rejection mixer uses the polyphase filter configuration to remove the image frequency. A 8th order bandpass filter (BPF) is used as a channel select filter, which is followed by Limiter & RSSI (Received

Signal Strength Indicator). A DLL based GFSK Demodulator is used to demodulate the received signal, which is followed by a clock and data recovery circuit which extracts the clock information from the received data.

In the transmitter, the input data is shaped using a digital Gaussian filter and then a sigma delta DAC is used to generate analog waveform of the data stream. 2-GFSK modulation is generated using open modulation technique, i.e. a Gaussian filtered analog signal is directly used to control VCO and generates GFSK modulation. Modulated waveform is then amplified to give out 4 dBm output using Power Amplifier. As Bluetooth is TDD system, a low loss RF switch is designed which connects antenna with Power amplifier or Low noise Amplifier based on the select signal.

2.4 Specification of transceiver

2.4.1 Noise Figure

Due to the internal noise of the receiver, the SNR at the output is degraded. Noise figure is used to specify how much internal noise in corrupting the incoming signal. Noise figure is defined as the ratio of SNR_{input} to SNR_{output} [15]. A SNR of 20 dB is needed at the output to satisfy the BER requirement of 10^{-3} as shown in figure 2.3 [12]. Assuming input sensitivity (S_{rec_in})of the transceiver is –80 dBm.

$$NF = (Srec\_in –(-174dBm +10\log_{10}B)) - SNR_{output}$$

$$= (-80\ dBm –(-174\ dBm + 60) – 20$$

$$= 34\text{-}20 = 14\ dB$$

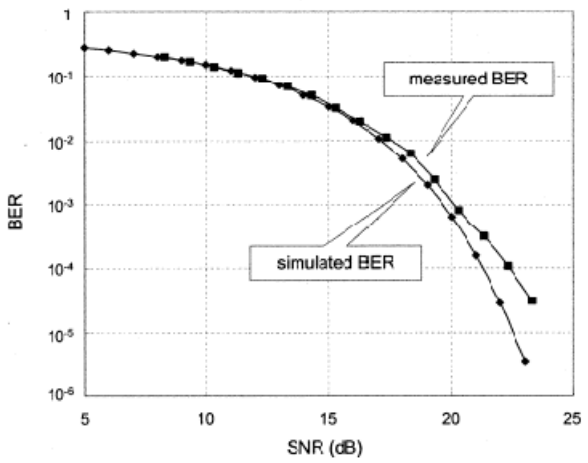


Figure 2.3 BER measurement for DLL based Demodulator [12]

2.4.2 Linearity

The required sensitivity should be achieved when the interference signal of -60 dBm are applied at 1Mhz and 2 Mhz away from the desired signal channel [1]. To achieve the required sensitivity, the input referred IM3 signal must be 20dB lower than the smallest possible wanted signal, -70 dBm and the input intercept point IIP3 is equal to

$$IIP3 = Pin + (Pin – IM3)/2$$

$$Or\ IM3 = 3 \times Pin – 2 \times IP3$$

Where Pin is the input power of an interference to the receiver in dBm [14]. The IM3 should be lower than the input referred noise floor of the system, Nin = -114 dBm

$$IM3 \leq Nin$$

$$(3 \times Pin – 2 \times IP3) \leq Nin$$

$$\therefore\ IP3 \geq (3 \times Pin\text{-}Nin)/2$$

$$\therefore\ IP3 \geq ((3 \times –60+114))/2$$

$$IP3 \geq -33\ dBm$$

2.4.3 Image rejection

According to the Bluetooth specification an image rejection of –20 dBm is required.

2.5 Specification of each block

Specification of each block is derived based on the specification of the receiver. To calculate the voltage gain of the block, source and load resistance of LNA is assumed to be 50Ω, for Mixer source is assumed to be 50Ω. while load as 1k. For filter and Limiter the source and load resistance are assumed to be 1kΩ. Bellow table shows the required specification of each receiver components.

Table 2-4 Transceiver Specification of Each Block

Component	Specification	Value
Receiver Front end	Sensitivity	-80 dBm
	SNR	20 dB
	NF	14 dB
	IIP3	- 33 dBm
	Image Rejection	-20 dB
	Power Gain (G)	31 dB
LNA	NF	3 dB
	Voltage Gain (Av)	12 dB
	Power Gain (G)	12 dB
	IIP3	-10 dBm
Mixer	NF	12 dB
	Voltage Gain (Av)	10 dB
	Power Gain (G)	-3 dB
	IIP3	-10 dBm
Filter	Center frequency	3 Mhz
	Bandwidth	1 Mhz
	Voltage Gain (Av)	-2.6 dB
	NF	6 dB
Limiter	Voltage Gain (Av)	30 dB

3. Switch

3.1 Introduction

A T/R-switch (SW) is one of fundamental RF front-end building circuits for realizing a wireless transceiver. As shown in figure 3.1 it solves the problem that occurs in the front-end of a radio transceiver of multiplexing between the transmitted and the received signal to the antenna in time division multiplexed systems like Bluetooth. Isolation, Insertion loss and power handling capability are three key figure of merit for measurement of switch's performance. GaAs switch are often used in practical wireless transceivers because the insertion loss of GaAs switch is much lower than that of CMOS.[17] [18] The large insertion loss of the CMOS switch is mainly due to the low-resistivity substrate and large on-state resistance of the CMOS transistors [20], [21], [22] which could reduced by proper sizing of transistors.

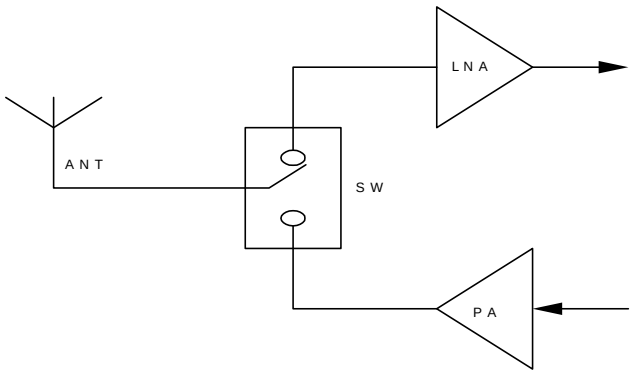


Figure 3.1 Application T/R Switch

There are two typical configurations used in CMOS switch design.

1. Series type switch

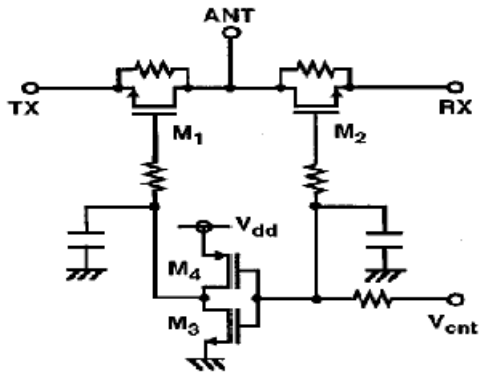


Figure 3.2 Series type Switch

In this figure 3.2, M1 and M2 form the series arm connecting Antenna with PA and LNA. M3 and M4 form the control circuit working in complementary fashion and thus consume no power. The insertion loss of this switch could reduce by increasing the transistors width, which reduces the on resistance but parasitic components also increase with increasing width, as a result the isolation of the switch becomes poor.

2. Series/shunt switch

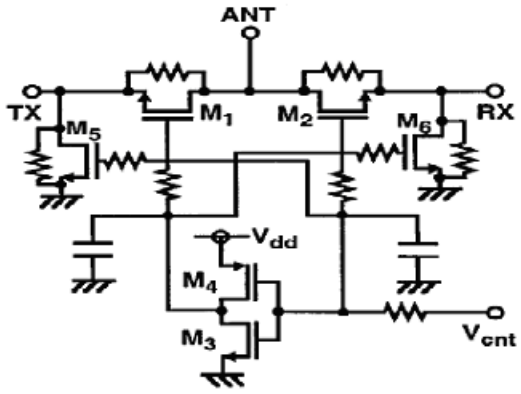


Figure 3. 3 Series/Shunt type Switch

Here M5 and M6 form the shunt pairs. For transmission, V1 goes high and V2 goes low, turning transistor M1 and M4 on and transistor M2 and M3 off. For receiving, V1 goes low and V2 goes high, turning M1 and M4 off and M2 and M3 on. M3 and M4 shunt the signal in receive- and transmit-mode respectively and thus increase isolation. Capacitance C1 and C2 allow DC biasing of the transmitting and receiving nodes. The purpose of resistance R1, R2 R3 and R4 is to improve DC bias isolation and has a value of about 10kΩ. This circuit has very good isolation in off-mode and was used in this transceiver designed. Through simulation an optimum width of 180μm was chosen which provides low insertion loss and good isolation.

3.2 Measurements

3.2.1 Insertion loss and Isolation

Loss is naturally an important parameter for a switch. Too high loss in on-mode will make the signal weak and too low loss in off-mode (isolation) will result in signal leakage. High loss in off-mode is especially important for switches separating the transmitter and the receiver while low loss in on-mode is important for switches before the LNA in the receiver. S parameter simulations were done to measure the Isolation

and insertion loss, which is shown in figure 3.4 and 3.5. An Insertion loss of –0.837 dB and isolation of –36dB was measured in post layout simulations.

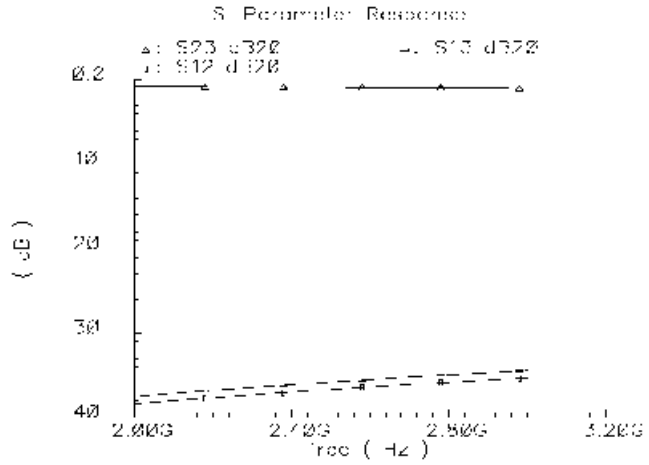


Figure 3.4 Insertion loss and isolation when LNA-Antenna are connected by switch

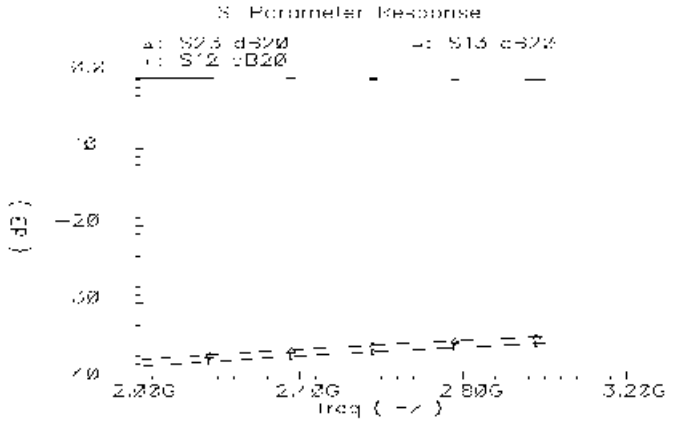


Figure 3.5 Insertion loss and isolation when PA-Antenna are connected by switch

3.2.2 Power handling capability

For low power signals the switch will work properly but as the power increase, the switching function will fail. As for the linearity this is critical for switches after the PA in the receiver. To measure how much power that can be delivered the 1dB compression point can be used (P1dB). It is defined as the input signal power that causes the small signal gain to drop by 1dB. The compression point is measured to be 12.3 dBm as shown in figure 3.6.

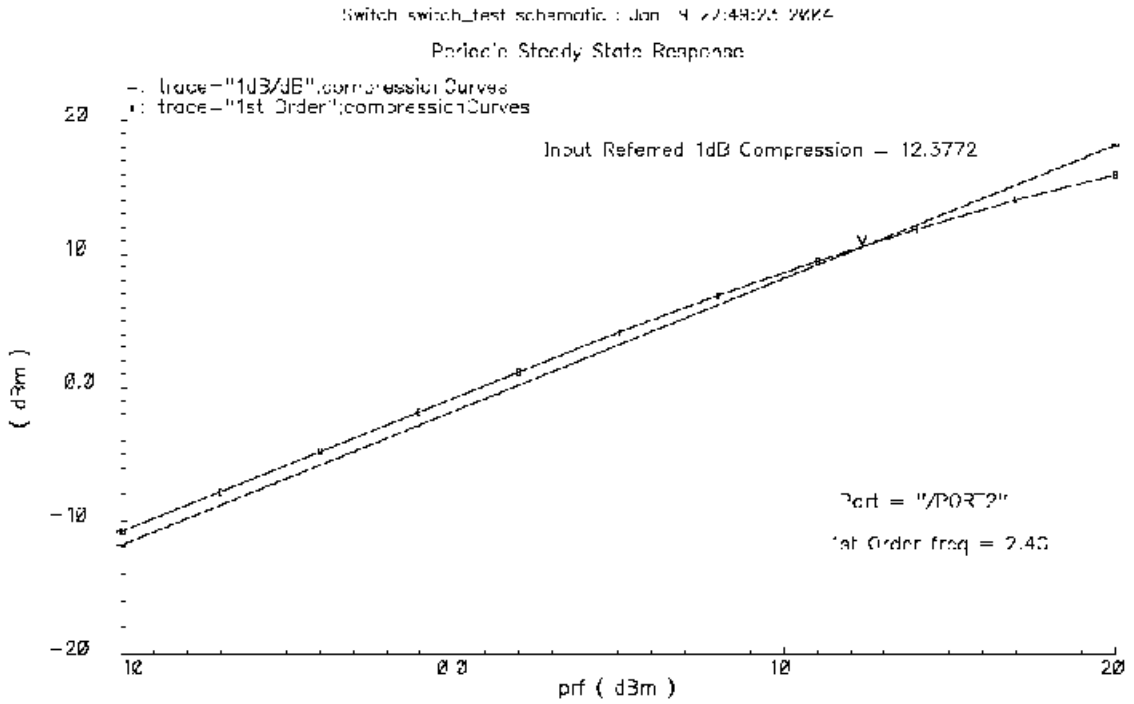


Figure 3.6 1dB compression point of the Switch

3.2.3 Noise figure

Finally, it is interesting to measure how much noise that is generated by a switch. Too much noise will corrupt the signal and make it hard to detect for systems after the switch. Hence, low noise is especially important for switches before the LNA in the receiver. For the frequency band of interest, the designed switch has a noise figure of 1.2 dB.

3.3 Summary

A switch design that allows the Bluetooth system to do TDD (time division duplexing) is presented in this chapter. The layout of this switch design is shown in figure 3.6. A brief summary of simulation results of switch is given in table 3.1

Table 3-1 Simulation Results of Switch Design

Specifications	Value
Insertion Loss	-0.837 dB
Isolation	-36.7 dB
Noise Figure	1.2 dB
1 dB compression	12.37 dBm
Area	105 μm x 95 μm

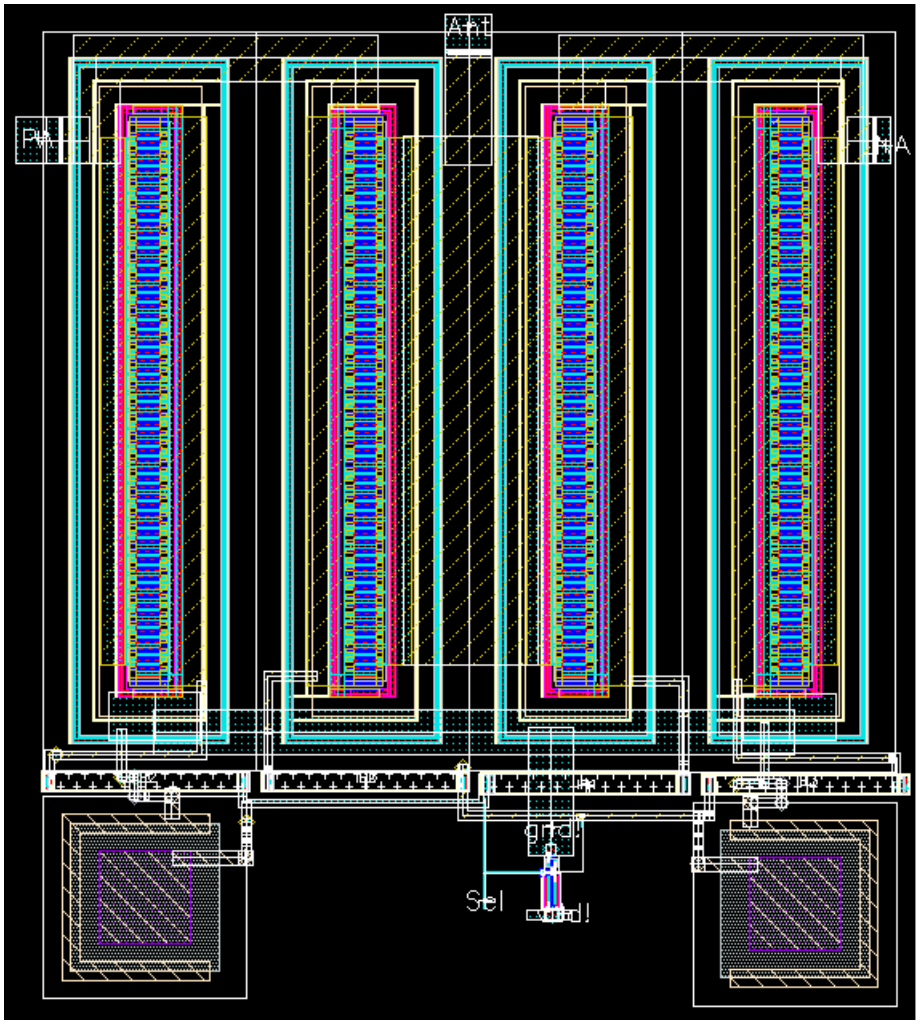


Figure 3.7 Layout of Switch

4. LNA

4.1 Introduction

A LNA (Low Noise Amplifiers) is a key component, which is usually placed at the front-end of a receiver system, immediately following the antenna. As we know from the Friis' formula (eq. 4.1) that the overall noise figure of the receiver front end is dominated by the first few stages [23].

$$NF_{rec} = \left(\frac{1}{G_{LNA}}\right)\left(NF_{subsequent} - 1\right) + NF_{LNA} \qquad \text{eq. 4.1}$$

where,

NF_{rec} = Noise Figure of the receiver

$NF_{subsequent}$ = Total Noise Figure of all subsequent stages

NF_{LNA} = Noise Figure of LNA

G_{LNA} = Gain of the LNA

From the above equation we could say that the noise of all the subsequent stages is reduced by the gain of the LNA and the noise of the LNA is injected directly into the received signal. Thus it is necessary for a LNA to boost the desired signal power while adding as little noise and distortion as possible so that retrieval of this signal is possible in the later stages in the system. Research in recent years on CMOS LNA design has investigated various features like topology, improvement of low noise figure, high power gain, and high linearity. All these features were considered while designing LNA. The requirements of LNA for the Bluetooth system are listed in the table bellow: -

Table 4-1 Characteristic and Specifications of an LNA

Characteristic	**Specification**
Noise Figure	NF < 3 dB
Gain	A_v > 12 dB
Centre frequency	*f =2.44 GHz*
Other characteristics	1.5V Power supply Low power consumption 0.18µm process 50 input impedance

4.2 LNA topology

There are several common objectives to be met in the design of CMOS low noise amplifiers like minimizing the noise figure of the amplifier and providing gain with sufficient linearity and providing a stable 50Ω input impedance which are discussed here.

4.2.1 Input impedance Matching

To present known resistive impedance to the external world, a number of circuit topologies [24] as shown in figure 4.1 were examined and we then narrowed the field of contenders.

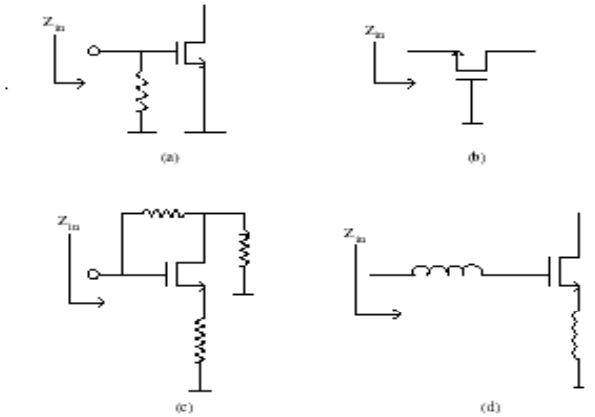


Figure 4.1 Common LNA architectures. (a) Resistive termination, (b) 1/gm termination, (c) shunt-series feedback, (d) inductive degeneration

The MOSFET input impedance is inherently capacitive, so providing a good match to a 50Ω resistance without degrading noise performance would appear to be difficult. Simply putting a 50Ω resistor across the input terminals of a common source amplifier as shown in figure 4.1(a) adds thermal noise while attenuating the signal ahead of the transistor. This produces unacceptably high noise figures. Another method as shown in figure 4.1(b) for realizing a resistive input impedance is to use a common-gate configuration since the resistance looking into the source terminal is 1/gm a proper selection of device size and bias current can provide the desired 50Ω resistance. But the noise figure of this configuration would be high for high frequencies due to the gate current noise of the transistor. The third configuration (figure 4.1(c)) uses a resistive shunt and series feedback to set the input and output impedances of the LNA. But

this has high power dissipation compared to others with similar noise performance due to the fact that shunt-series amplifiers of this type are naturally broadband, and hence techniques that reduce power consumption through LC tuning are not applicable. It also requires on-chip resistors of reasonable quality, which are generally not available in CMOS technologies. We found that the fourth architecture shown in figure 4.1(d), employing inductive source degeneration is the best method. With such an inductance, a real term in the input impedance can be generated without the need of real resistances, which degrade the noise performance. Tuning of the amplifier input then becomes necessary, making this a narrow band approach, which is favorable for our application.

$$Z_{in} = j\omega(L_g + L_s) + (1/j\omega C_{gs}) + (g_m L_g / C_{gs}) \qquad \text{eq. 4.2}$$

The first two components Z_{in} that form the imaginary part of the impedance would resonate out at the desired frequency (2.44Ghz) leaving only real part $g_m L_g/C_{gs}$. Thus the components are to be sized so as to get the value of gm, Lg and Cgs so that the real part of input impedance is equal to 50Ω.

For maximum power delivery conjugate impedance matching between antenna and LNA is needed. But this won't always give a minimum noise figure. So some intentional mismatching is done to get Noise Figure near to NF_{min}. This matching type of impedance matching is called Noise matching.

4.2.2 Noise Figure

From the Friis' formulae we know that the Noise Figure of any network is dominated by the first stage. So for the Cascode Topology used for the LNA, the Transistor M1 would dominate the noise figure. Noise Figure of this Cascode LNA is given by the equation 4.3 [15].

$$NF = 1 + \frac{2}{3 g_m R_s} \qquad \text{eq. 4.3}$$

The expression which gives a relationship between the optimum transistor width Wopt which would provide the minimum Noise Figure for given power dissipation is given by Lee[25].

$$Wopt = \frac{1}{3\omega L C_{ox} R_s} \qquad \text{eq 4.4}$$

Using this relationship the first guess for the width of the Transistor M1 which would give the minimum Noise Figure could be made then other inductors and capacitors are chosen so as to get a good input and output match.

4.3 Implementation and Design Flow

In order to obtain the desired Noise figure an initial guess for the width of M1 transistor is made using the equation 4.4. The TSMC provides the table of the width of the transistor and minimum NF that transistor could achieve for give biasing based on equation 4.4[25]. This table is used make the first guess for the width of the transistor. The width of transistor M2 is set as same width as M1. The Lg and Ls are sized according to eq 4.2. so as to get a 50Ω input match. Similarly Ld and Cd is set so as to get a 50 Ω output match. The circuit is then simulated using SpectreRF .The PSS and Pnoise analysis is done to see if the Noise figure specs are met. If they are not then individual noise contribution of each component is checked and they are resized to reduced their noise contribution. This is done iteratively till the required noise figure is achieved. Once the required Noise Figure is achieved the various other parameter like input /output VSWR , Gain, Stability, linearity, etc are measured. The variation in biasing Vgs voltage affects the Noise figure a lot. So a bandgap temperature reference was created which would provide a stable voltage irrespective of temperature and supply voltage variation.

Special care needs to be taken while doing the layout of the LNA so that routing capacitances and resistance affects the performance of the circuit as little as possible. Most of the routing is done on top most metal layers as they have minimum resistance. Figure 4.2 shows the layout of the LNA.

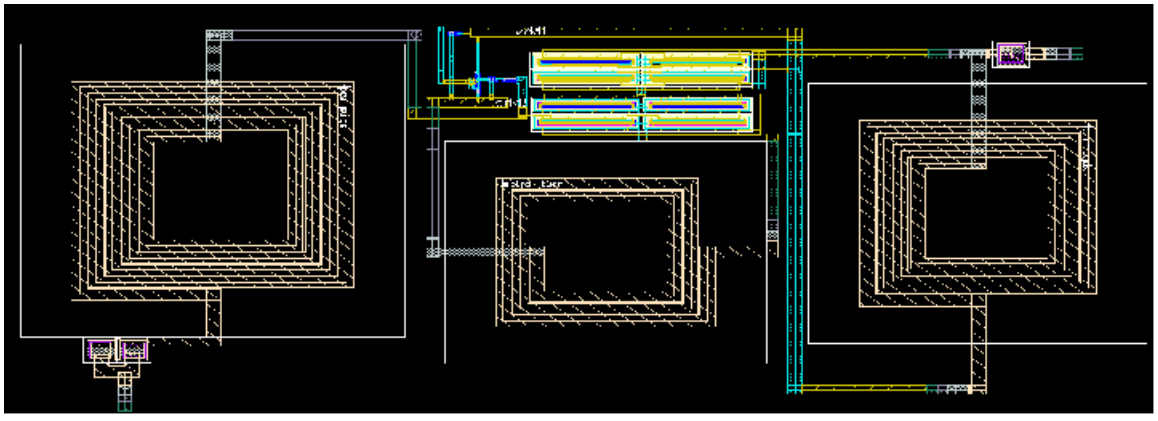


Figure 4.2 Layout of LNA

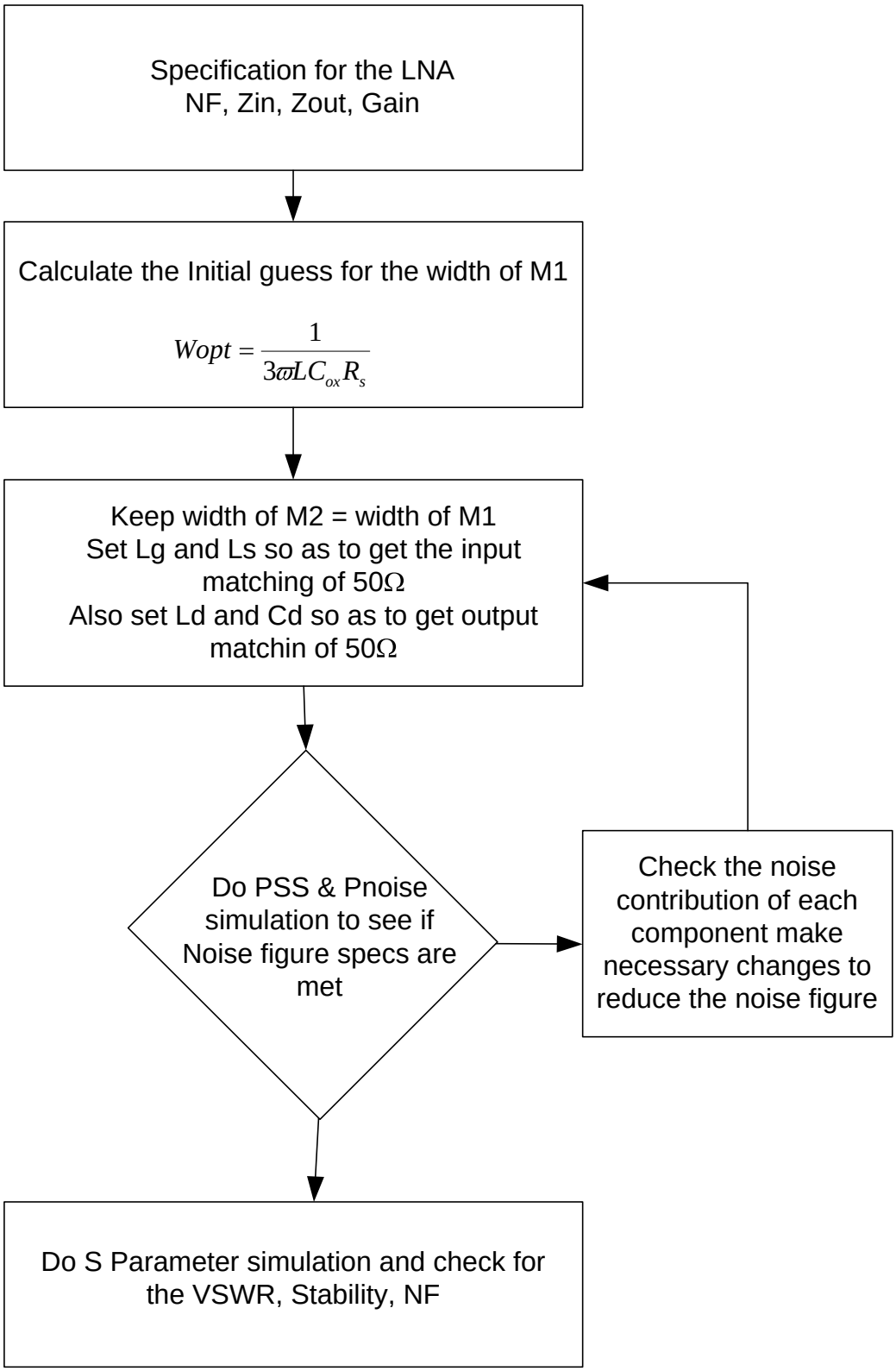


Figure 4-3 Design flow of LNA design

4.4 Simulation

The LNA was simulated in SpecteRF and ADS. The S-parameter of LNA were extracted and S-parameter analysis was done to measure the stability, gain, VSWR and Noise figure of it. Also PSS (Periodic Steady State) Analysis was done to measure the linearity (IP3) of LNA design.

4.4.1 Input/Output Matching

The first constraint on the LNA is to assure that the input impedance matches the source impedance, i.e. the LNA presents a purely resistive load of 50Ω to the antenna, in order to maximize the power transfer. In order to verify this, we simply plot the input and the output VSWRs as shown on Fig 4.4 . For input, we obtained a VSWR of 1.41 and an output VSWR of 1.8 was achieved.

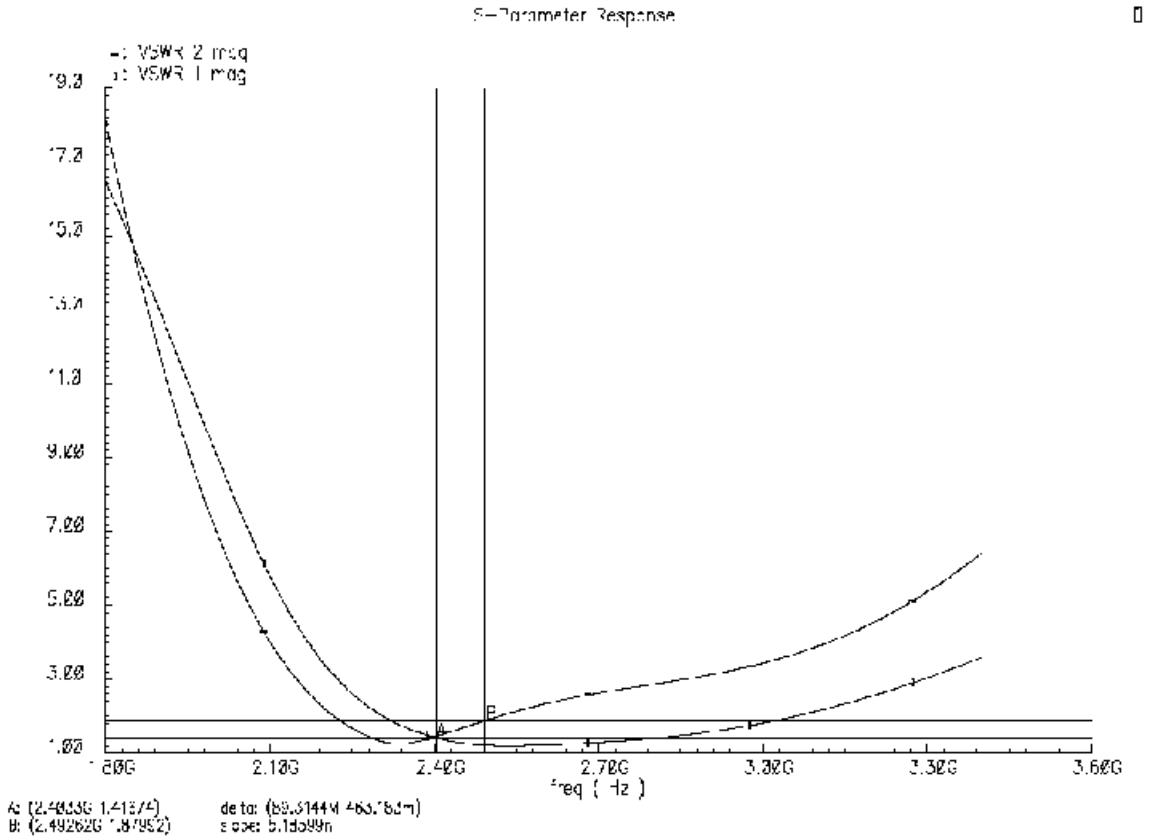


Figure 4.4 Input and Output VSWR of LNA

4.4.2 Gain

The following plot (Fig 4.5) shows the gain as a function a frequency. A gain of 12.57 dB was obtained from the LNA design.

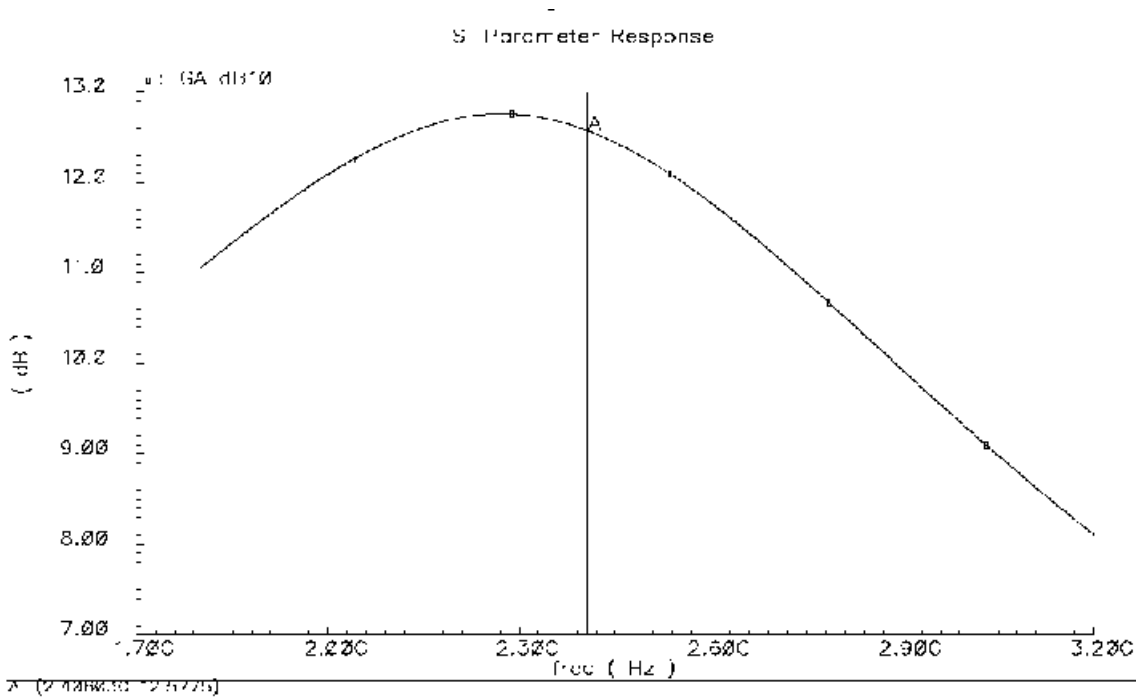


Figure 4.5 Gain Plot of LNA design

4.4.3 Noise Performance

A noise figure of 2.3 dB was achieved by doing noise matching and trying to get the NF curve close to the Nfmin as shown in bellow figure.

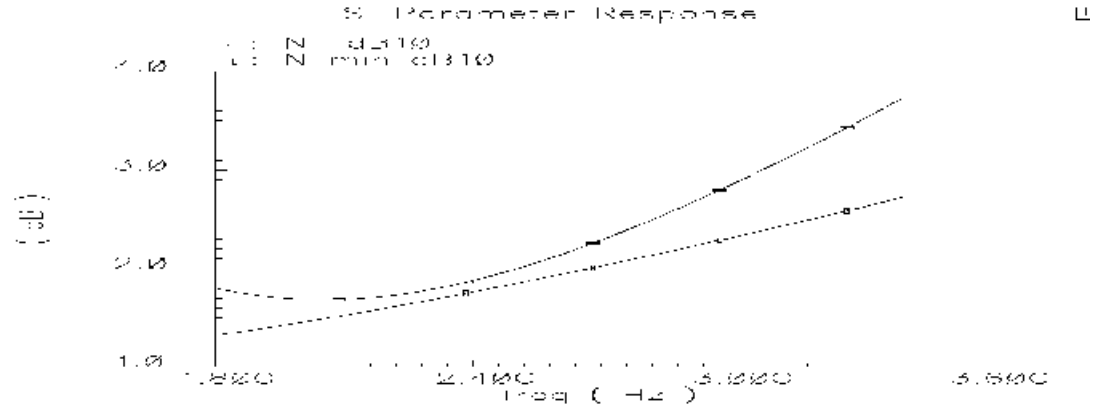


Figure 4.6 Noise Matching of LNA

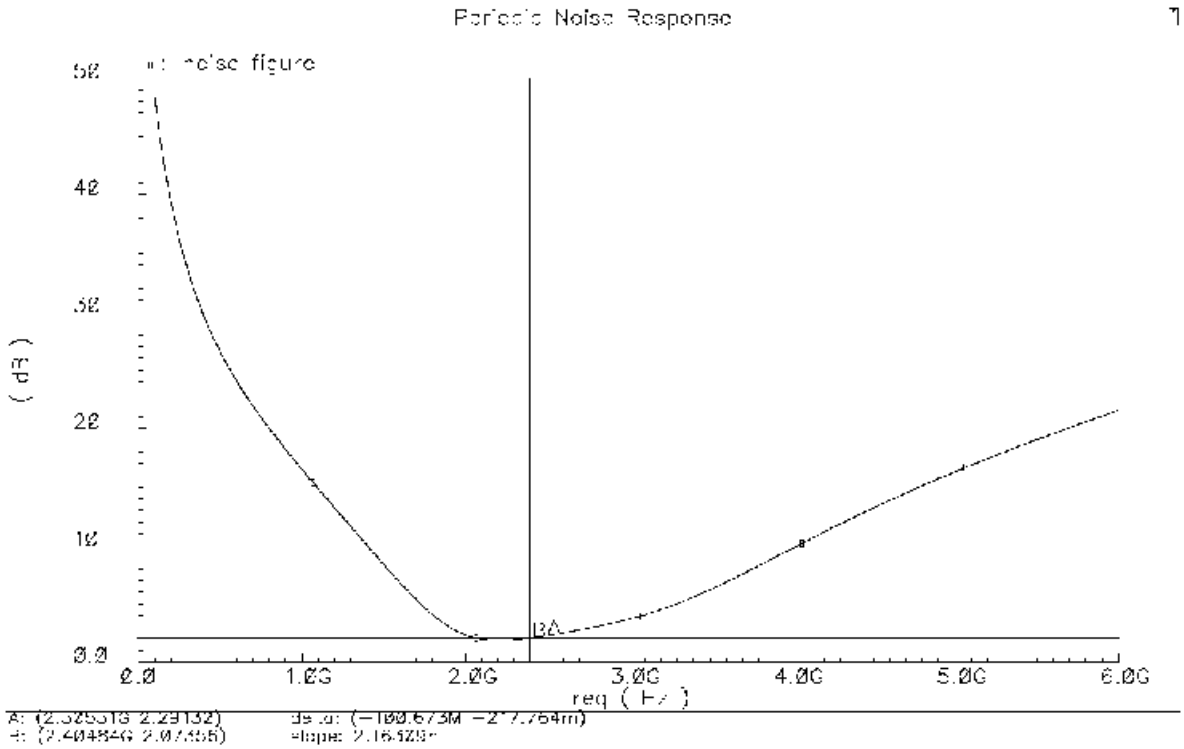


Figure 4.7 Noise Figure Measurement using Periodic Noise Analysis

4.4.4 Linearity

IP3 measurement is done to measure the linearity of the LNA design. Two tone used were 2.4Ghz and 2.41Ghz. As shown in figure 4.8 the LNA design is able to achieve an IP3 of 4.04 dBm

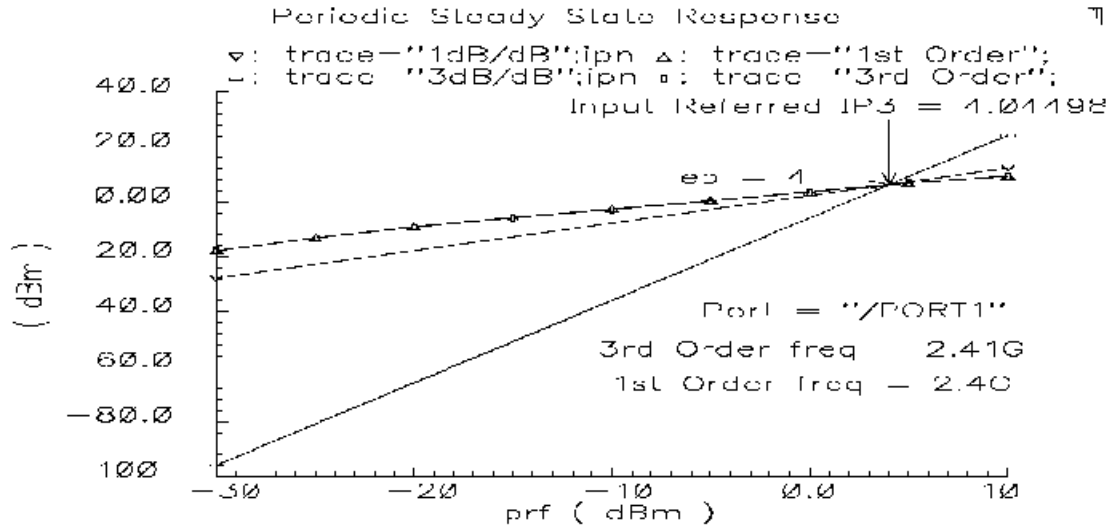


Figure 4.8 IP3 measurement of the LNA design

4.5 Summary

A Low Noise Amplifier design, which satisfies all the specification, is presented in this chapter. The following table summarizes the LNA design.

Table 4.2 Summary of Performance of LNA design

Center Frequency	2.45 GHz
Ga (gain)	12.57 dB
Noise Figure	2.3 dB
IIP3	+4.04 dBm
Input VSWR	1.41
Output VSWR	1.8
Area	1100μm x 500μm

5. Mixer

5.1 Introduction

A Mixer acts as a frequency converter, which converts the signal from one frequency (usually f_{rf}) to another (typically f_{if}) with minimum loss of the signal and minimum noise performance degradation. The Mixer performs the frequency translation by multiplying the two signals, which is possible due to some components of Mixer operating in nonlinear region [15]. As shown in eq1, two signals having frequency ω_{rf} and ω_{lo} when

$$\left(A\cos\omega_{rf}\right)\left(B\cos\omega_{lo}\right)=\frac{AB}{2}\left(\left(\cos\left(\omega_{rf}-\omega_{lo}\right)\right)+\cos\left(\omega_{rf}+\omega_{lo}\right)\right) \qquad \text{eq. 5.1}$$

multiplied gives sum and difference frequency. The difference frequency is normally called intermediate frequency ω_{if}, which is a lower frequency on which latter stages of receiver chain works.

Various Mixer topologies are broadly classified as Passive and Active Mixers. Passive Mixer works on the switching principle and they don't provide any gain. While Active Mixer uses the nonlinear characteristics of the devices to multiply signals and they normally provide some gain. Various different types of Active Mixer based on the concept of balancing are classified as bellow.

Unbalanced Mixer

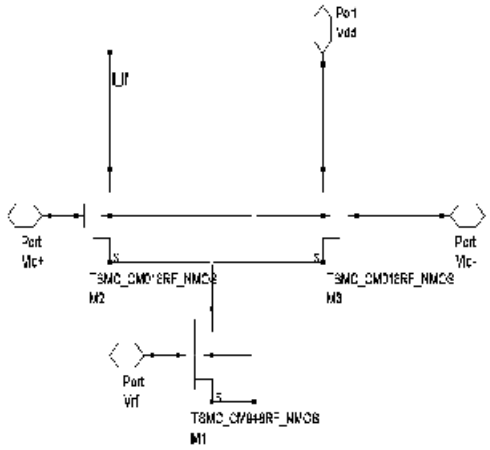


Figure 5.1 Unbalanced Mixer

It is the simplest form of Mixer, where output (IF signal) is taken from on branch only. This IF signal is described by the equation

$$V_{if}(t) = A_{rf}\cos\omega_{rf}t \times G_o\left(\frac{1}{2} + \sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_0 t\right) \qquad \text{eq. 5.2}$$

The DC component of the LO signal is multiplied with RF signal to produce a scaled product at the output, this causes the components of RF signal to appear at the output. This phenomenon is called RF feed-through and is undesirable.

Single Balanced Mixer

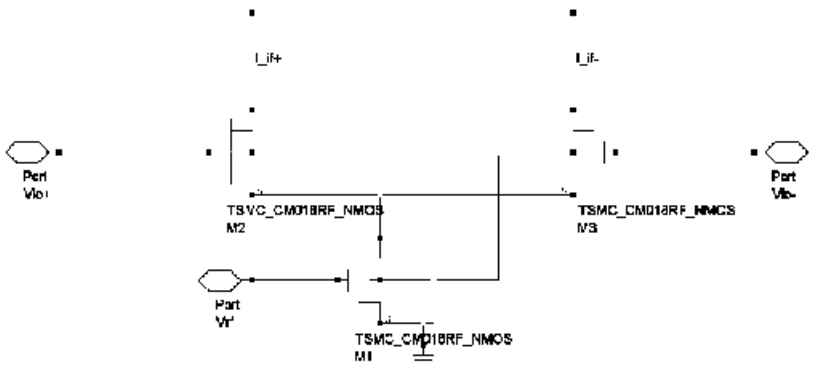


Figure 5.2 Single Balanced Mixer

Here output is taken from both the branches (I_if+ and I_if-) giving the differential output which can be written as

$$V_{if}(t) = A_{rf}\cos\omega_{rf}t \times 2G_o\left(\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_0 t\right) \qquad \text{eq. 5.3}$$

As the differential output is taken from both the branches the dc component (rf feed-through) of both branches cancel out each other. In addition, it can be shown that the even harmonics of RF frequency and frequency components at $n\omega_{lo}$ from the RF input won't show up in the output. But the frequency components at $n\omega_{lo}$ from the LO input, where n is an integer, will propagate to the output. This is called LO

feed-through. Although it has a simple design, it provides moderate gain and low Noise Figure [14]. However the design has low 1dB compression point, port-to-port isolation, low ip3 and high input impedance.

Double Balanced Mixer

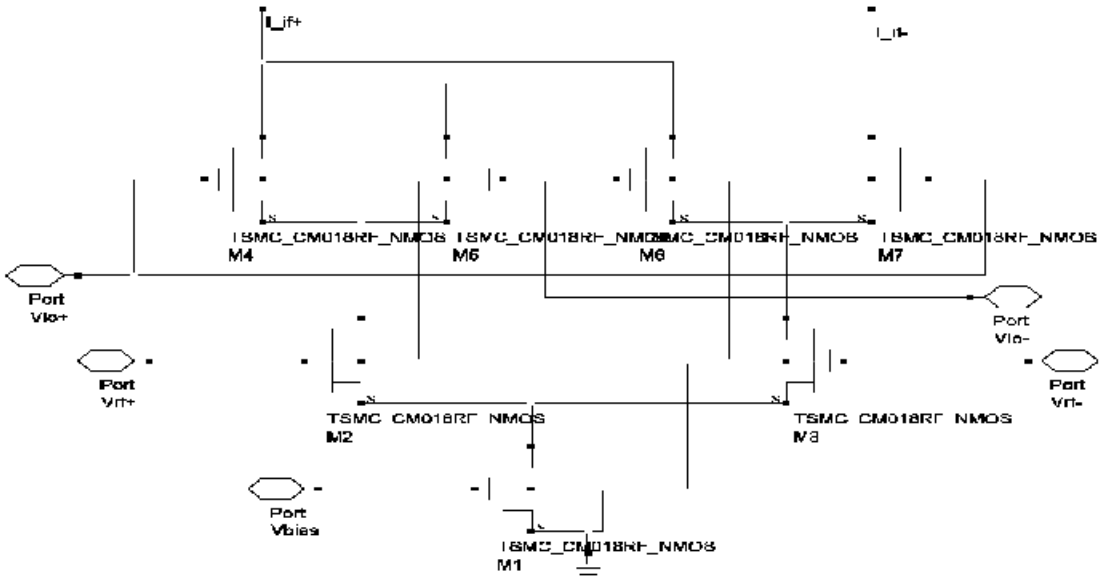


Figure 5.3 Double Balanced Mixer

By combining two of the single balanced mixer as shown in figure a double balanced mixer is formed. It is also called Gilbert mixer. A double balanced mixer rejects both RF and LO feed-through. This configuration has the highest port-to-port isolation and provides high gain and low noise figure. This mixer needs a differential RF input, but most of the Antennas available are single ended and to convert those single ended output to balanced output a balun, which can not be integrated on single chip. Addition of the balun in system would increase the overall system cost.

Also as a low IF type of receiver topology was chosen for this Bluetooth Transceiver, it also suffers from the problem of suppressing the image/mirror signal [26]. As shown in figure if a wanted is situated on f_c, the mirror frequency is at f_c-2f_i then Mixer would gives a frequency component on f_i for f_x =f_c and f_x=f_c-2f_i, i.e. both mirror and wanted signal are down converted to same frequency and its tough to distinguish between them. So image frequency has to be suppressed. Filter needed to suppress this image

signal needs to have a high Q value, which are tough to integrate. A special kind of Mixer configuration called Hartley Mixer, which uses the complex IQ mixing, can alleviate this problem of image frequency[28].

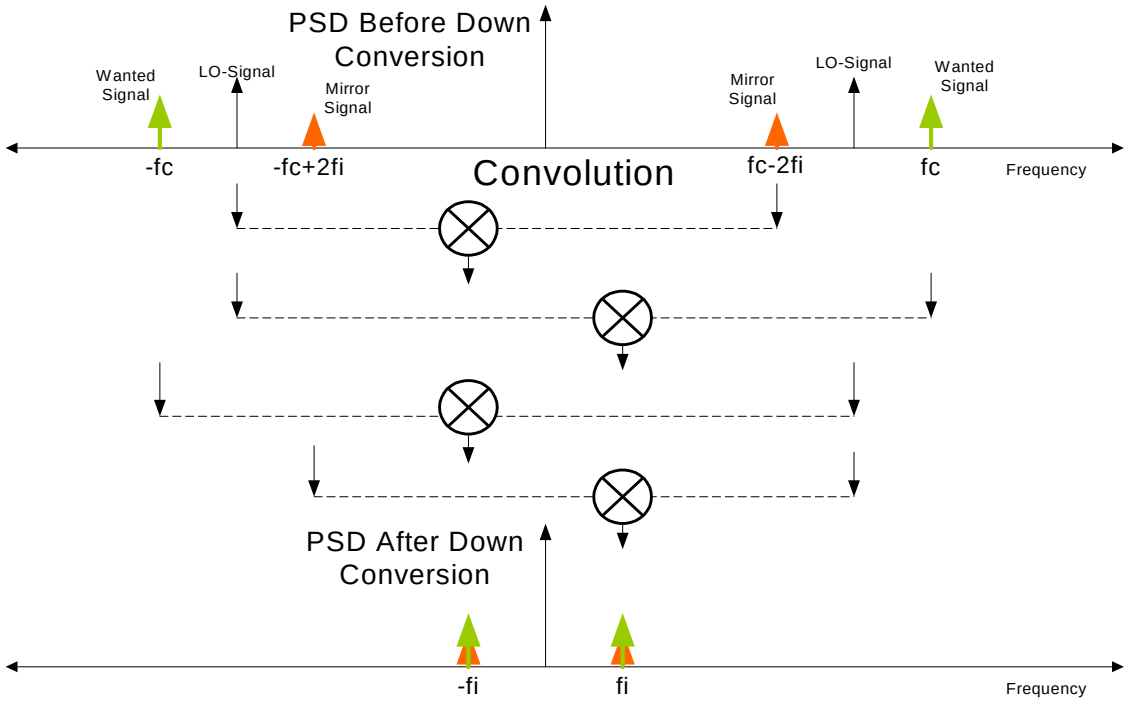


Figure 5.4 Effect of Image frequency

5.2 Hartley Mixer

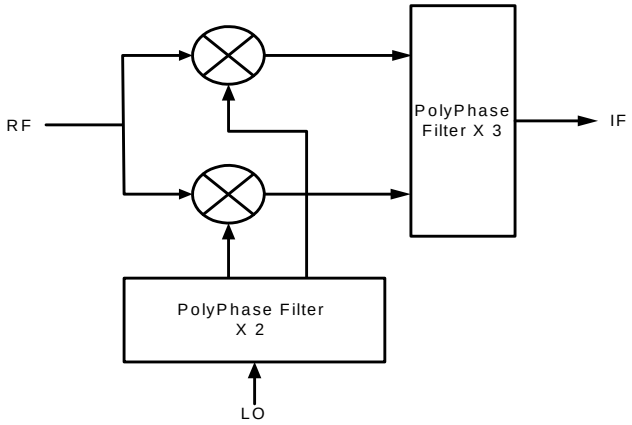


Figure 5.5 Hartley Mixer Configuration

Above filter consist of the two Poly-Phase filters, which are basically Hilbert filter. A Hilbert filter creates a bandpass response by translating a lowpass prototype with the shift transform, $s \rightarrow (s+\omega 0)$, so the

frequency response is no longer mirrored about zero frequency, and the desired frequency may lie in the passband, while the image frequency lies in the stop-band [30]. With this in mind, a Hibert filter may be synthesized to null the image while passing the desired frequency. This polyphase filter may be used in two places in a wireless receiver: to generate balanced quadrature phases from a single phase, and to reject the image.

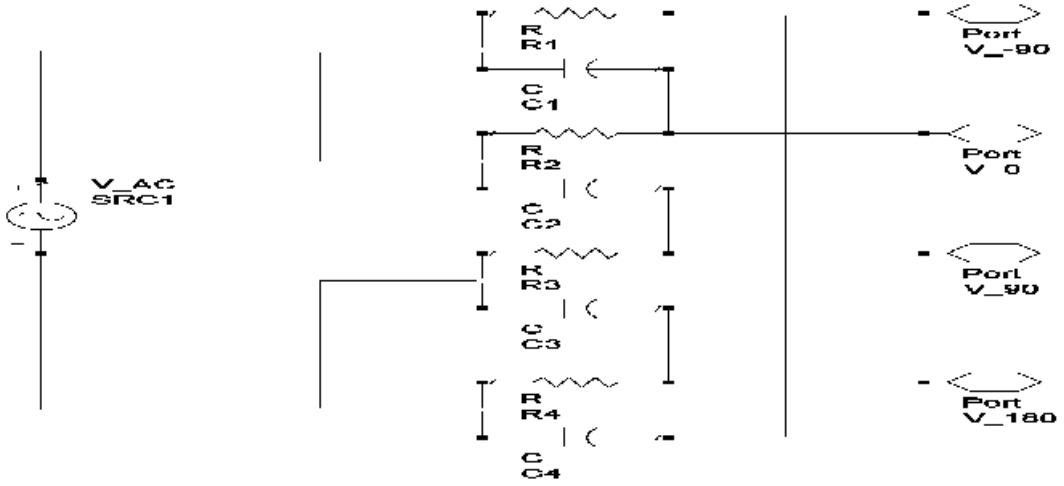


Figure 5.6 Polyphase filter configured as Phase shifter

Figure 5.6 shows how differential quadrature phases are generated from a differential input. The differential signal is decomposed into two equal amplitude quadrature sequences, one clockwise and the other counterclockwise. When the input signal frequency is at the RC pole, the polyphase rejects the clockwise sequence and only the counterclockwise sequence comprising perfect balanced quadrature survives at the output.

For image rejection, the image and desired signals are first downconverted by quadrature LO phases, which maps them to the same frequency but into two opposite sequences. This follows from the trigonometric identities

$$\sin(\omega_{LO} \pm \omega_{IF})t \times \sin \omega_{LO} t = \frac{1}{2}(+\cos \omega_{IF} t - \cos(2\omega_{LO} + \omega_{IF})t) \rightarrow +\frac{1}{2}\cos \omega_{IF} t \qquad \text{eq. 5.4}$$

$$\sin(\omega_{LO} \pm \omega_{IF})t \times \cos \omega_{LO} t = \frac{1}{2}(+\sin \omega_{IF} t - \sin(2\omega_{LO} + \omega_{IF})t) \rightarrow +\frac{1}{2}\sin \omega_{IF} t \qquad \text{eq 5.5}$$

Then a polyphase filter tuned to ω_{IF} following the mixers passes the desired signal but nulls the image.

5.3 Implementation and Design flow

For this Bluetooth Transceiver design a Low IF of 3MHz was chosen. At such a low IF frequency and with channel spacing of 1 MHz, problem of image frequency becomes severe. Also Bluetooth specification has requirement of suppression of image frequency by –20dBm. To take into account of all these specification, a Hartley Mixer, which is a type of IRM (Image Rejection Mixer) was designed. By using this the requirement of the Bandpass filter's input range is relaxed by 15 dB.

Two Single Balanced mixers were used to mix the RF signal with 90' phase shifted IQ LO signal. Single Balanced was chosen as it accepts a single ended input available from the LNA. It also consumes less power compare to Double balanced mixer and still give good Noise Figure and IP3.

Depending upon the required Noise figure and power consumption requirements choose the size of the transconductor M1 which converts the RF voltage to current which is mixed by the M2-M3 switches to produce the IF signal output [27]. Sizes of the M2-M3 are chosen such that they contribute least Flicker noise. Then Load transistor M4 and M5 are sized so as give-required conversion gain as per equation 3.

$$Gc = \frac{4}{\pi}\left(g_{m1} \times R_L\right) \qquad \text{eq 5.6}$$

Then circuit is simulated in SpectreRF simulator to see if the specification of Noise Figure, Conversion Gain and IP3. If any of the requirements are not fulfilled then needed resizing of the components is done and this done iteratively till all requirements are fulfilled. After fulfilling all the required specifications peripheral circuits like biasing network and input/output matching network are designed. The whole circuit then verified to make sure that it still fulfills all specifications. The whole design procedure is shown in figure 5.7.

Quadrature LO signals are generated using two stage LO polyphase filter network as shown in figure. The poles of the two stages is set at 2.44Ghz ± 20% to take into account for the process variations. Similarly IF polyphase filter network was designed with poles at 3 Mhz , 3 Mhz + 20% and 3 Mhz – 20%.

IF combiner circuit that could sum up the quadrature output of the polyphase filter was designed. This IF combiner circuit contains two differential amplifiers that adds the quadrature components of the

differential outputs from the IF polyphase filter network. A CMFB (Common Mode Feedback) circuit was added to ensure a fixed dc level of the output.

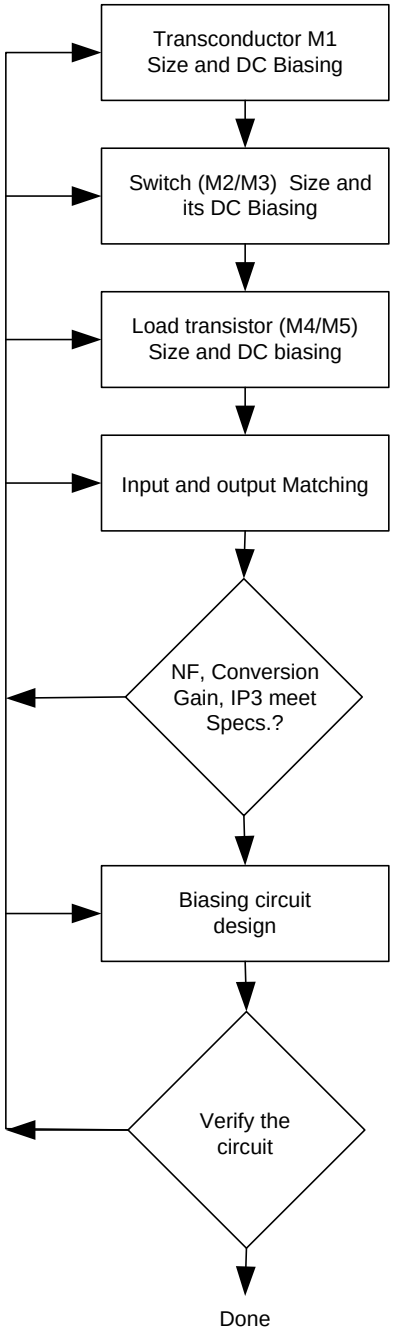


Figure 5.7 Mixer Design Flow

5.4 Simulation

5.4.1 Linearity

A highly linear mixer is desired as it helps to reduce the effects of adjacent channel interference. The linearity of mixer is measured with IP3 or Input referred Third order intercept. IP3 simulations were done in ADS simulator. As shown in figure 5.8 the mixer design achieves the IP3 value of –14.4 dBm

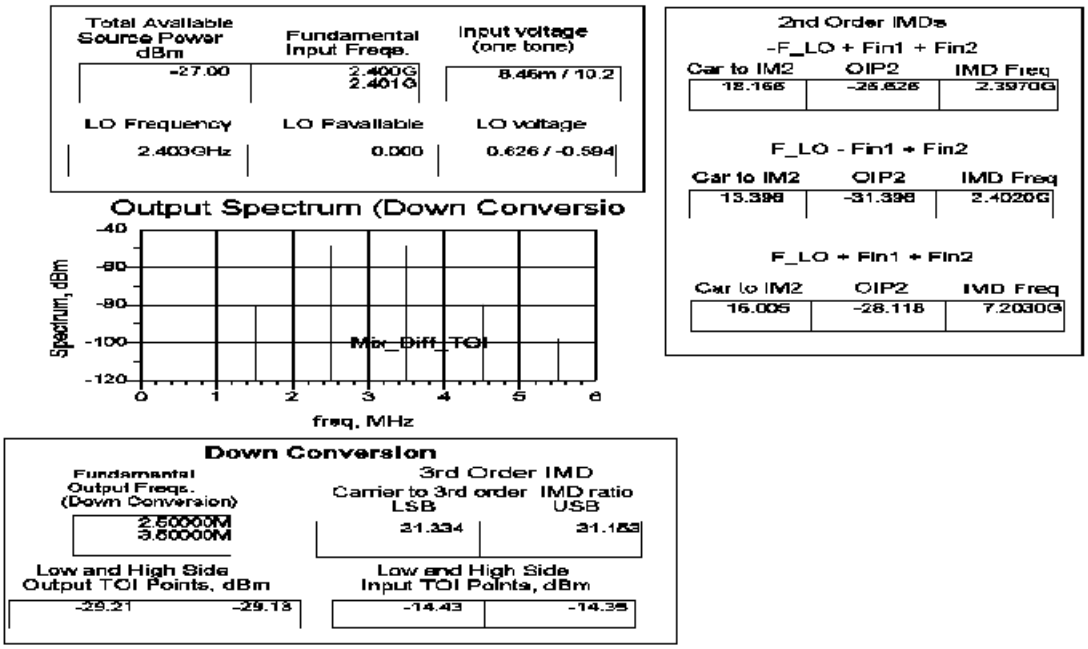


Figure 5.8 IP3 simulation result of Mixer

5.4.2 Conversion Gain

As shown in figure 5.9 the periodic steady state simulation shows that the mixer design achieves the gain of 7.4 dB and a noise figure of 16 dB.

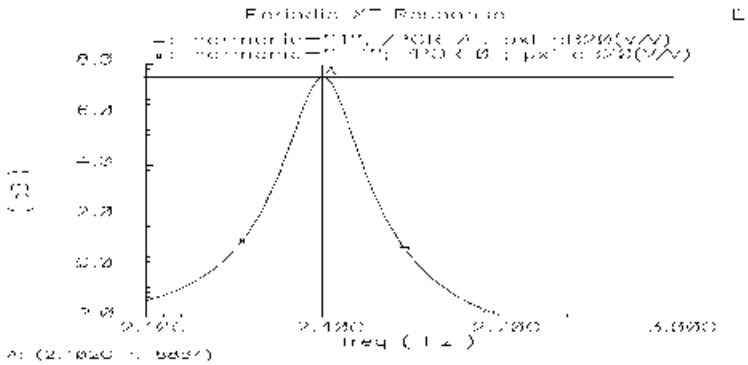


Figure 5.9 Conversion Gain of Mixer

5.5 Summary

A Mixer design, which satisfies all the specification, is presented in this chapter. The following table summarizes the Mixer design.

Table 5.1 Performance of Mixer Design

Intermediate Frequency	3 MHz
Conversion Gain	7.4 dB
Noise Figure	16 dB
IIP3	-14 dBm

6. Filter

6.1 Introduction

As shown in bellow figure 6.1, along with the desired signal, the mixer also down converts unwanted adjacent signals. So a channel select filter, which could remove/suppress the unwanted adjacent signals and would only allow to pass the desired information signal, is connected after the mixer.

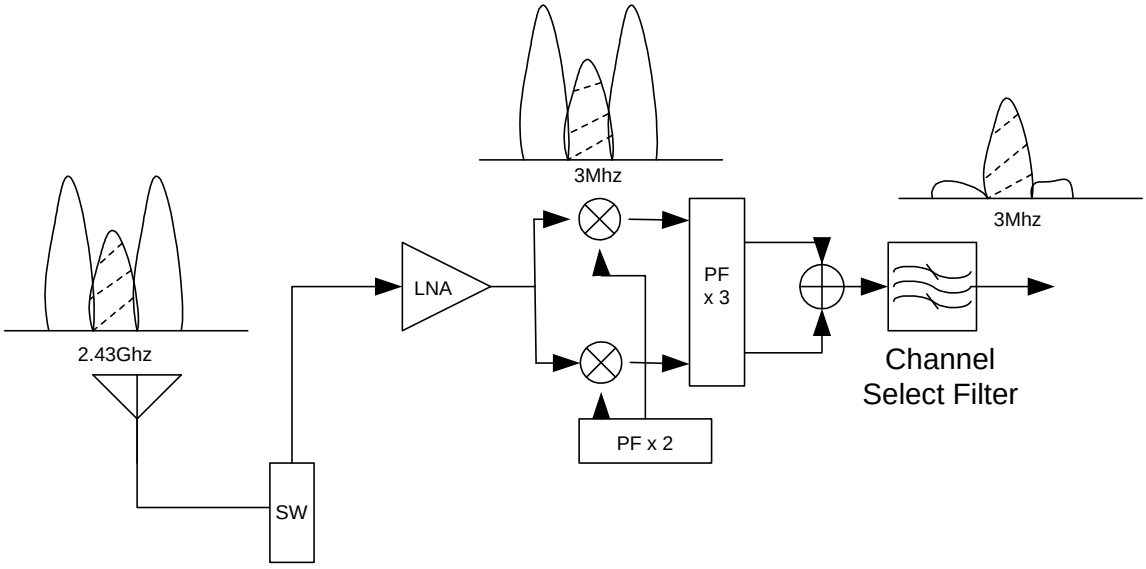


Figure 6.1 Why Channel Select filter in needed in transceiver

This channel select can be realized with either analog or digital circuit. The digital circuit tends to be more complex and would need an additional high resolution ADC. This would increase the overall system power consumption. Analog filters can be realized with the switched capacitor or OTA-C circuits. The switched capacitor circuits are easier to design but they need a clock signal operating at a much higher frequency than the center frequency. It is tough to design switch operating a very low voltage (1.5V). Moreover the switched capacitor circuits suffer from the clock-feed through problems. While for OTA-C (Operational Transconductance Amplifier) filter no switches or clock signals are required. And with tuning circuit they provide a very stable characteristic and could overcome the effects of parasitics, temperature and process variation.

Designing a higher order filter by cascading the biquads is quite popular due to its modularity of structure and simplicity of design [31]. The biquads are second order filters and they form the basic sections in the cascaded structures. The basic building blocks of the OTA-C filters are shown in figure.

The amplifier configuration shown in figure 6.2 has gain

$$k = \frac{Vo}{V1 - V2} = \frac{g1}{g2} \qquad \text{eq 6.1}$$

The ideal integrator in Figure 6.3 has the characteristic of

$$H(s) = \frac{Vo}{V1 - V2} = \frac{1}{s(C1/g1)} \qquad \text{eq 6.2}$$

A lossy integrator is given in Figure 6.4, which has the lowpass transfunction

$$H(s) = \frac{Vo}{V1 - V2} = \frac{g1}{sC1 + g2} \qquad \text{eq 6.3}$$

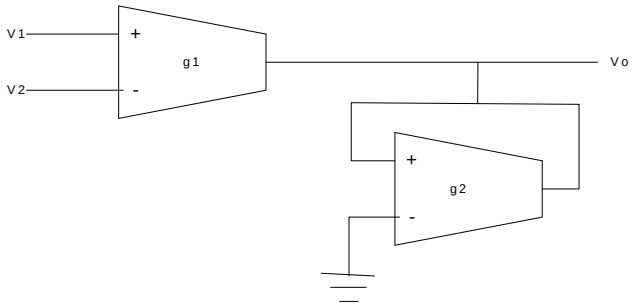


Figure 6.2 Amplifier

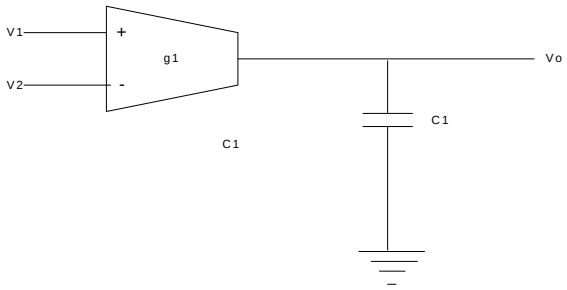


Figure 6.3 Ideal Integrator

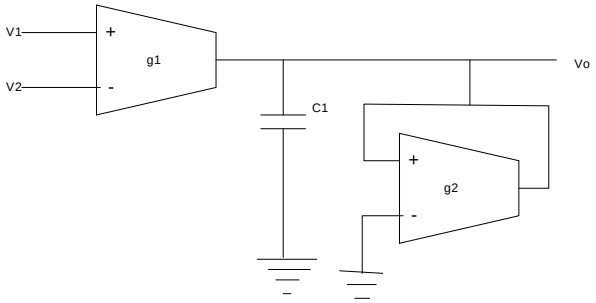


Figure 6.4 Lossy Integrator

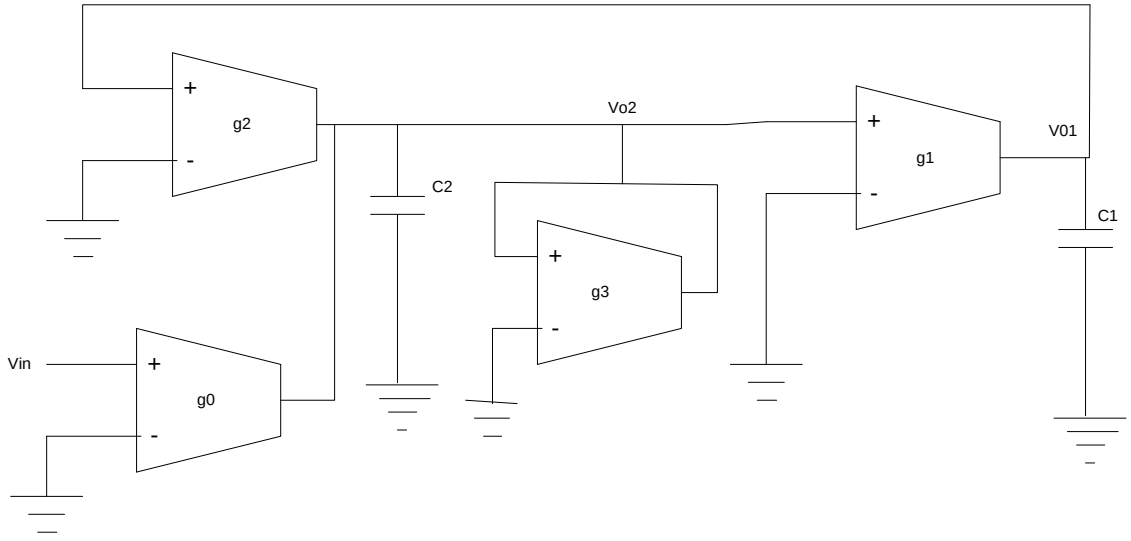


Figure 6.5 Thomas-Tow gm-C filter

The OTA-C structure shown in figure 6.5 consisting of an ideal integrator and a lossy integrator in a single loop is a biquads and is considered to be an OTA-C equivalent of the Thomas-Tow (TT) active RC biquads [3]. This TT filter structure has a very simple structure, a very low sensitivity and low parasitic effects. For given input Vi, the transfer functions of the circuit at output Vo1 and Vo2 can be given by

$$H_{LP}(s) = \frac{Vo1}{Vin} = \frac{-g0g1}{s^2C1C2 + sg3C1 + g1g2} = \frac{-K_{lp}\omega_0^{\,2}}{s^2 + s(\omega_0/Q) + \omega_0^{\,2}} \qquad \text{eq 6.4}$$

$$H_{BP}(s) = \frac{Vo2}{Vin} = \frac{sg0C1}{s^2C1C2 + sg3C1 + g1g2} = \frac{-K_{bp}(\omega_0/Q)s}{s^2 + s(\omega_0/Q) + \omega_0^{\,2}} \qquad \text{eq 6.5}$$

$$\omega_0 = \sqrt{\frac{g1g2}{C1C2}} \qquad \text{eq 6.6}$$

$$Q = \frac{1}{g3}\sqrt{\frac{g1g2C2}{C1}} \qquad \text{eq 6.7}$$

$$K_{lp} = \frac{g0}{g2} \qquad \text{eq 6.8}$$

$$K_{bp} = \frac{g0}{g3} \qquad \text{eq 6.9}$$

As it can be seen from the equation 6.4 and 6.5 that if output is taken form Vo1 then TT biquads has a low pass transfer function. And if the output is taken from the Vo2 node then it has a bandpass transfer function. Thus by proper choice of Transconductances and Capacitor value desired center frequency and Q value could be attained. And by cascading many such stages would create an nth order filter. A balanced structure of the TT bandpass OTA-C filter is shown in figure 6.6.

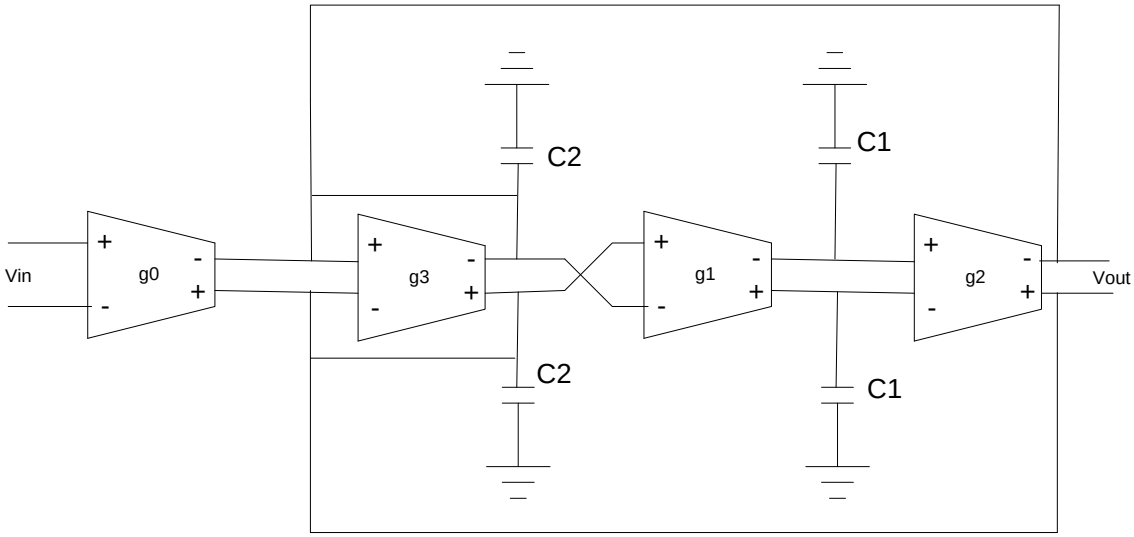


Figure 6.6 Balance structure of Thomas-Tow bandpass OTA-C filter

6.2 Implementation and design flow

For the designed Bluetooth transceiver a filter needs to have a bandwidth of 1 Mhz, center frequency at 3Mhz and an attenuation of more than 20dB @ fc ± 1MHz . These requirements are satisfied by 16^{th} order bandpass filter which is created by cascading 8 TT biquads.

Designing a bandpass filter for channel selection is tough, as it has to operate over a wide input voltage range at low supply voltage of 1.5V [2]. The gm cell designed used is based on the Krummenacher's design [34]. Here the linearizing transistors M3 and M4 are connected to the differential input voltage, which helps to increase the linearity of the gm cell. In this configuration the transistors M3 and M4 always remain in linear/ triode region, which is highly desirable. The Transconductance generated by this gm cell can be given by the equation

$$Gm = \frac{4k1k3\sqrt{I}}{(k1+4k3)\sqrt{k1}} \qquad \text{eq 6.10}$$

where

$$k1 = \frac{\mu nCox}{2}\left(\frac{W}{L}\right)_1 \qquad \text{eq 6.11}$$

$$k3 = \frac{\mu nCox}{2}\left(\frac{W}{L}\right)_3 \qquad \text{eq 6.12}$$

Thus the transconductance of the gm cell could be varied by changing the current flowing through the gm cells. To maximize the input and output range, the bias voltage of the input terminal Vbias was chosen as

$$Vbias = Vdd - \left(Vdsatp + \frac{Vpp}{2}\right) \qquad \text{eq 6.13}$$

$$Vpp = Vdd - (Vth + Vdsatp + Vdsatn1 + Vdsatn5) \qquad \text{eq 6.14}$$

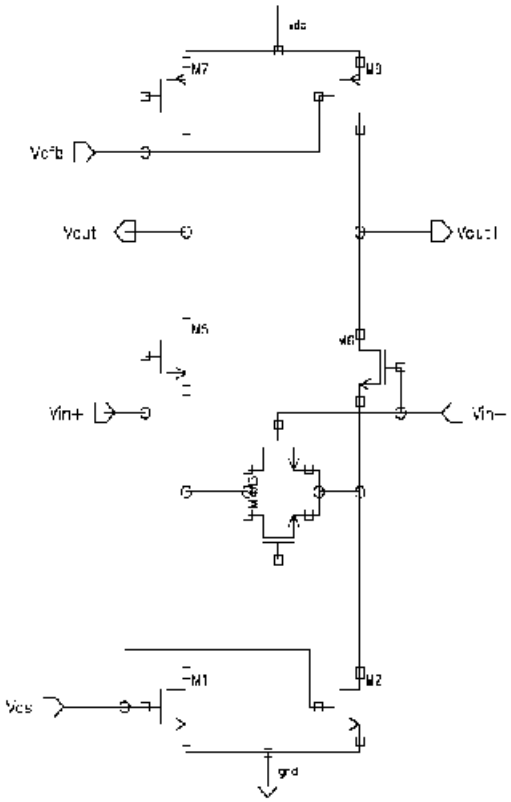


Figure 6.7 OTA Cell

The common-mode feedback circuit (CMFB) for the gm cells is shown in figure 6.8.

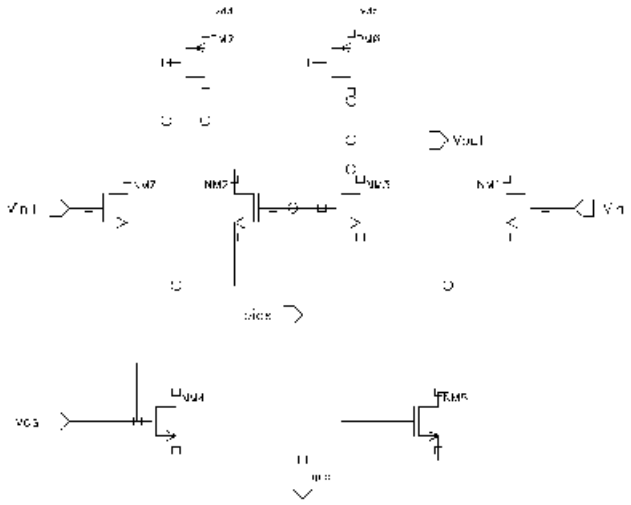


Figure 6.8 CMFB Circuit for OTA cell

The CMFB circuit was designed so as to get Vpp nearly to 500mV and Vbias is around 1V. The gain of the gm cells g1 and g2 were kept equal. And values of the Capacitors C2 and C1 are set so as to get at center frequency of 3Mhz and bandwidth of 1Mhz. A low pass configured TT biquads was kept at the end, as the roll off on the high side of the bandpass configuration was not to the required level. The figure 6.9 shows the AC plot of the Filter's Output.

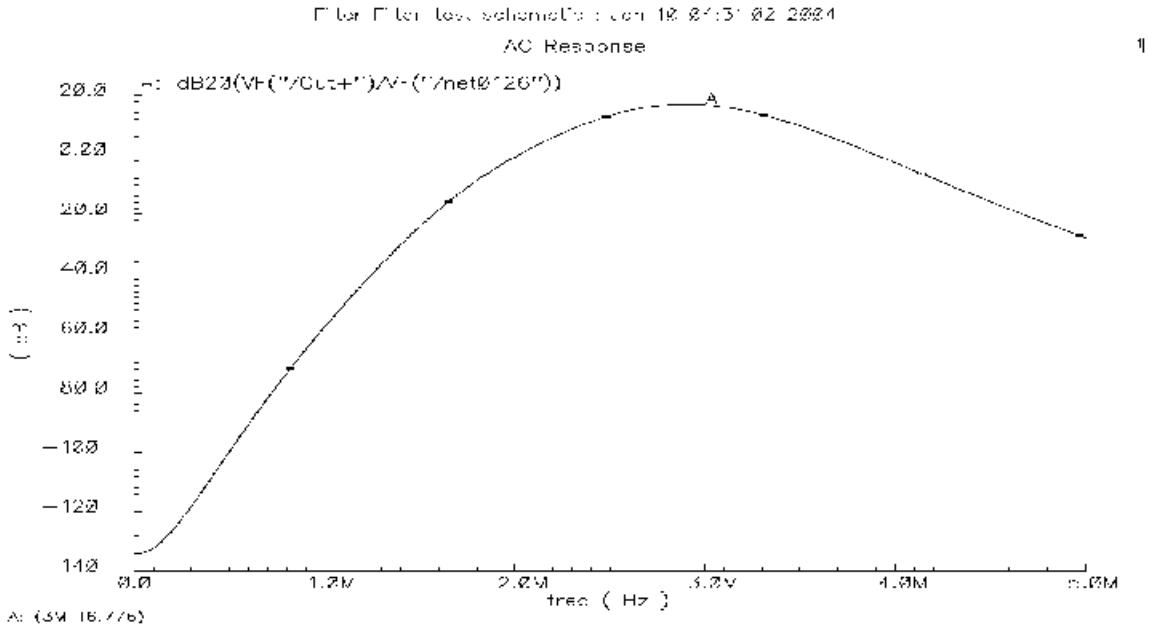


Figure 6.9 AC response of Filter

6.3 Summary

In this chapter a power optimized Filter design, which provides a gain of 16.77 dB and having a bandwidth of 1 Mhz, is presented. The designed filter provides a suppression of –20 dB at 2/4 MHz frequency.

7. GFSK Modulator And Demodulator

7.1 Introduction

A Gaussian Frequency Shift Keying modulation has been chosen as modulation technique for the physical layer of Bluetooth. GFSK is a kind of continuous phase frequency shift keying (CPFSK) method having a constant envelope, which allows the use of relatively nonlinear power amplifiers. Also as the waveform produced by the GFSK modulator is continuous in phase even at the edges of the symbols, this system has some containment in frequency, which allows for more channels to be accommodated in a given bandwidth. Also as in GFSK modulation the information is carried in frequency, the additive noise doesn't impact in a direct manner.

GFSK is a kind of FSK modulations were data is transmitted by varying the frequency of transmission. The basic FSK modulation can be given by following equation :-

$$s(t) = \sqrt{\frac{2E_s}{T}} \cos\left(2\pi f_c t + \frac{h\pi(t - nT)}{T} + \phi_n \right) \qquad \text{eq. 7.1}$$

where,

Es = Energy per Symbol

T = Symbol duration

fc = Carrier Frequency

h = Modulation index

A pure GFSK suffers from the phase discontinuity and hence occupies more bandwidth. An FSK spectrum can be made more compact by removing these phase discontinuity. Filtering the incoming data sequence conserves the bandwidth and generates a continuous phase FSK signal, which is given by following equation.

$$s(t) = \sqrt{\frac{2E_s}{T}} \cos\left(2\pi f_c t + 2\pi h \sum a_n q(t + nT)\right) \qquad \text{eq 7.2}$$

Instantaneous frequency of this signal can be given by

$$f(t) = 2\pi f_c t + 2\pi h \sum a_n g(t + nT) \qquad \text{eq 7.3}$$

where, g(t) = dq/dt

This CPFSK signal would cause ISI (Inter Symbol Interference) if modulating signal g(t) is not a nyquist pulse. For GFSK modulated signal the filter having Gaussian characteristics filters input data sequence and this signal is mathematically represented by bellow equation.

$$s(t) = \sqrt{2E_s T}\cos\left(2\pi f_c t + \theta(t)\right) \qquad \text{eq 7.4}$$

$$\text{where} \quad \theta(t) = \sum a_i \pi h \int_{-\infty}^{t+iT} g(u)du \qquad \text{eq 7.5}$$

According to the Bluetooth Standard a modulator and demodulator capable of fulfilling following modulation and demodulation specification given bellow needs to be designed.

Modulation = GFSK

Modulation index = 0.32 ± 1%

BT = 0.5 ± 1%

Bit rate = 1Mbps

Frequency accuracy better than ± 1ppm.

7.2 GFSK Modulation techniques

As GFSK is a kind of FSK modulation, so techniques used in FSK modulation can be used here. The two methods which could generate GFSK modulated waveforms are

7.2.1. Direct Modulation

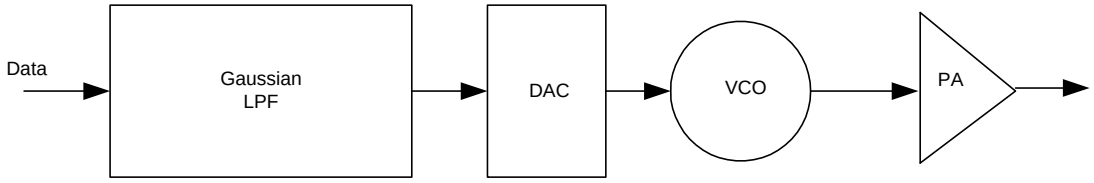


Figure 7.1 Direct GFSK modulations with VCO

Here data is data is Gaussian filtered and fed to VCO (Voltage Controlled Oscillator) which generates the frequency modulated signal. This GFSK VCO modulator architecture as shown in figure is simple. Here required modulation index of 0.35 is generated by the VCO, but this modulation index tends to drift over time and due to temperature variation.

7.2.2. Quadrature Modulation

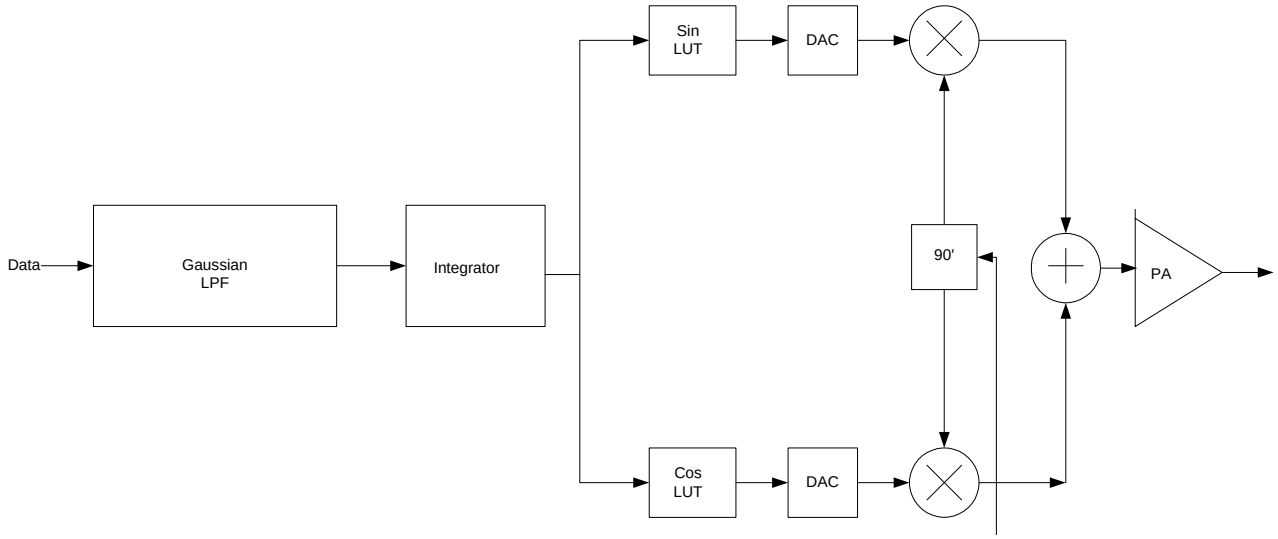


Figure 7.2 Quadrature GFSK Modulations

Quadrature Modulation is based on the IQ kind of modulation concept. Here data is Gaussian filter and then integrated. This integrated data is then used to look up in the Sine/Cosine Look up table, which stores the modulated data. This type of quadrature modulation doesn't suffer from the effects of temperature as in direct modulation. But it uses twice as much hardware and proves to be costly. So direct modulation technique was chosen for the designed Transceiver.

7.3 Gaussian filter design

In GFSK modulation, a filter having Gaussian impulse response is used as pre filtering of the symbols prior to continuous phase modulation. This is used to control the bandwidth of the modulated signal. The Gaussian filter is characterized by its BT product. (B is the –3dB bandwidth and T is the symbol period = $1/f_{symbol\_rate}$). Lower the BT product, narrower the modulation bandwidth and higher the inter-symbol interference (ISI). The impulse response of Gaussian filter is analytically given by

$$h(t) = \frac{1}{\sqrt{2\pi}\sigma T}\exp\left(\frac{-t^2}{2\sigma^2 T^2}\right) \qquad \text{eq 7.6}$$

$$\text{where } \sigma = \frac{\sqrt{\ln(2)}}{2\pi BT}$$

Design of Gaussian filter

The Gaussian filter was first designed and simulated in Matlab to ensure that designed filter provides the needed filtering. Bluetooth uses the BT= 0.5 which when inserted in equation gives the standard deviation of the Gaussian filter's impulse response.

$$\sigma = \frac{\sqrt{\ln(2)}}{\pi} = 0.2206 \qquad \text{eq 7.7}$$

Using this value and equation a FIR filter with 20 tap was created. The frequency and time response of the designed filter is shown in figure bellow.

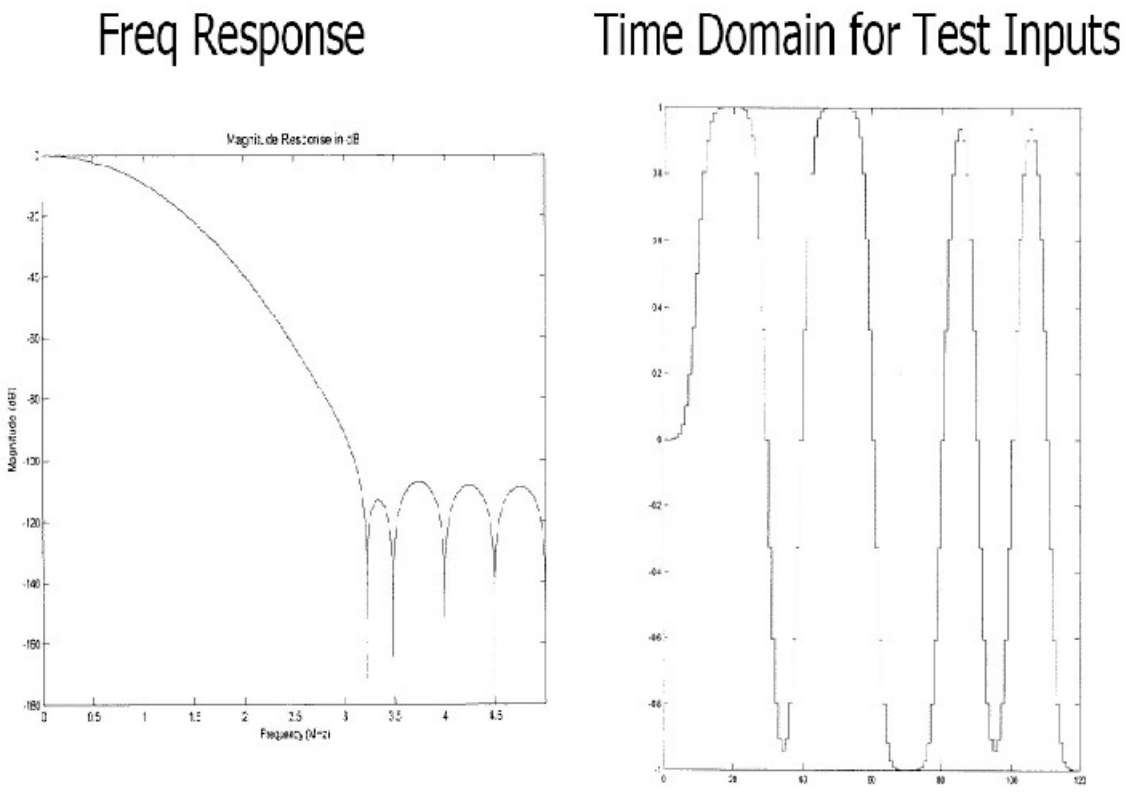


Figure 7.2 Frequency and Transient response of Gaussian Filter

The coefficient of filter shown in table were quantized to 9,8,6 bits and simulated again in Matlab to see the effects quantization. As shown in figure 7.3, 9 bit compares well to the theoretical waveform, but there aren't many 9-bit adders in synthesis library so it wasn't chosen. 8bit loses some of this resolution, but still

has general form and there is not much degradation in performance when coefficients were quantized by 8 bits, hence 8 bits quantization was chosen.

Table 7.1 Table of Filter Coefficients

Tap #	Ideal	9-Bits	8-Bits	6-Bits
1, 20	1.422742E-05	0	0	0
2, 19	0.000166769	0	0	0
3, 18	0.000919642	0	0	0
4, 17	0.003622688	0.00390625	0	0
5, 16	0.111519468	0.01171875	0.0078125	0
6, 15	0.027777459	0.2734375	0.03125	0.03125
7, 14	0.056944433	0.05859375	0.0546875	0.0625
8, 13	0.096983628	0.09765625	0.09375	0.9375
9, 12	0.137970298	0.13671875	0.140625	0.125
10, 11	0.16444886	0.1640625	0.1640625	0.15625

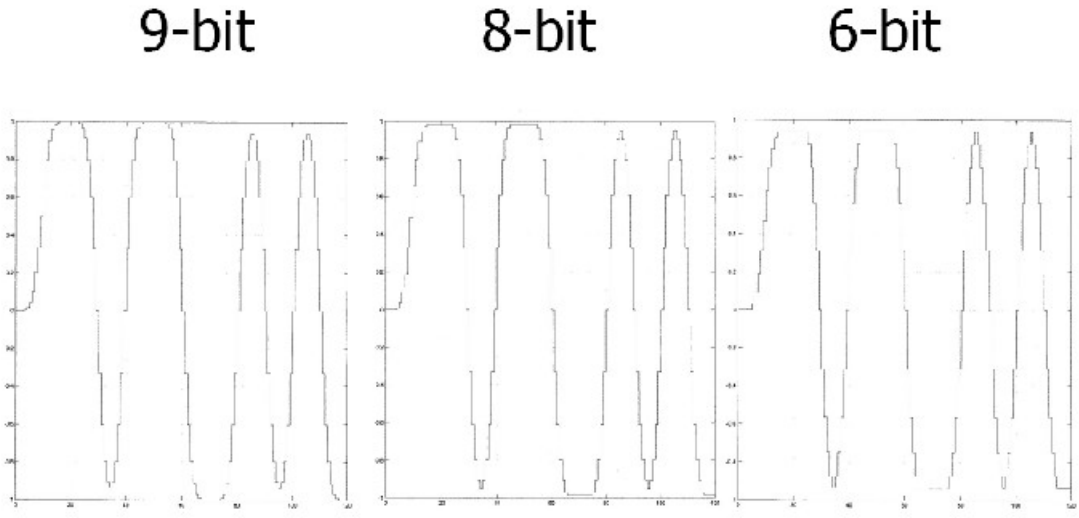


Figure 7.3 Transient Response of Gaussian filter with 9/8/6 bit quantization

Figure 7.4 shows the top level implementation of the Gaussian filter. The architecture of the Gaussian filter was designed to have as much pipelining as possible and reduce the number of adders. Present design uses only 3 Adders. The control unit consist of 10 stage state machine that enables counters, registers and provides the sample clock. Gauss Filter shown in figure is basically mux, which selects appropriate coefficient based on current count and bit. Figure 7.5 shows the comparison between the Matlab and Verilog outputs. The two output differ at the initialization as Matlab tends to start at the mid range value

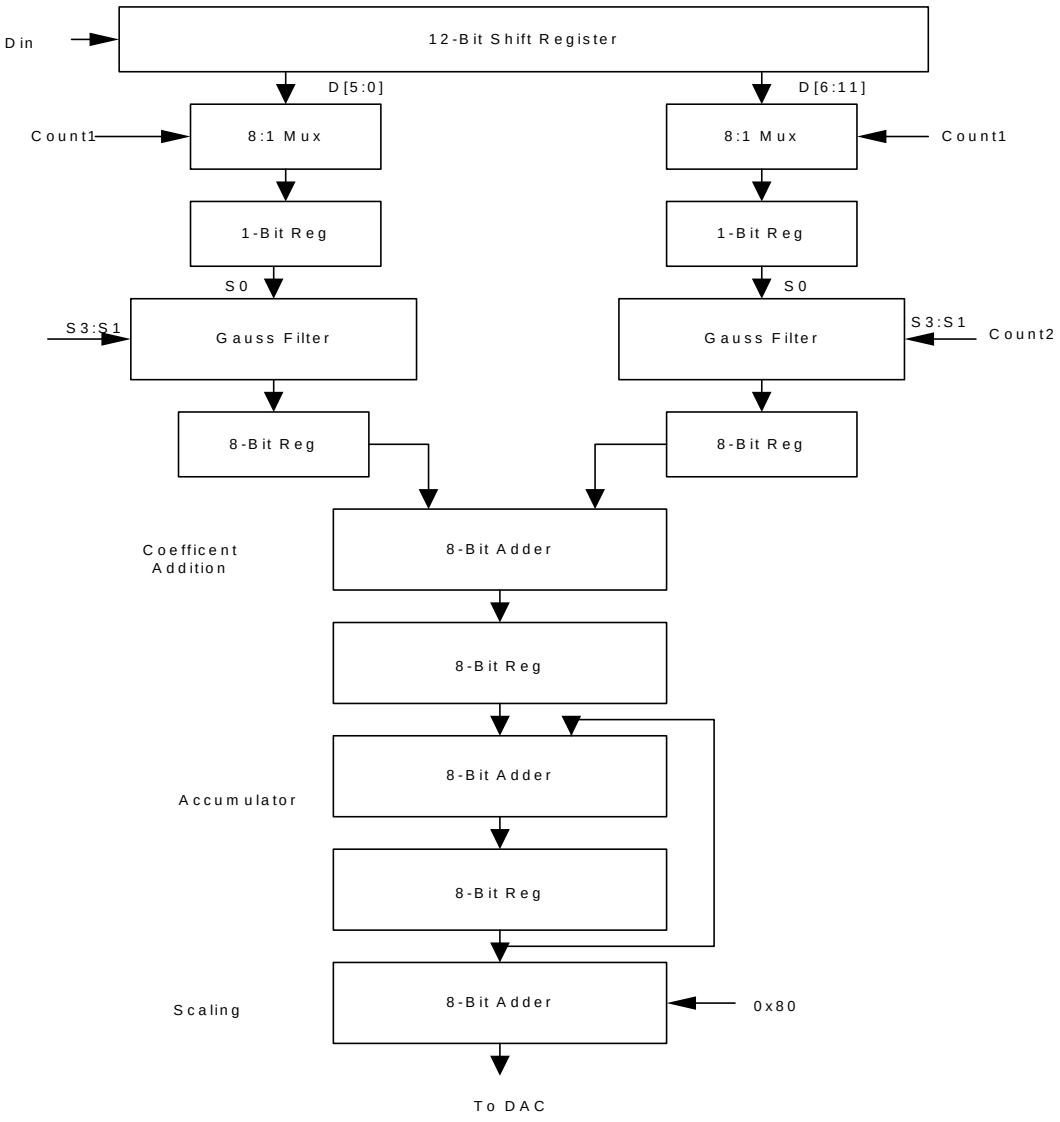


Figure 7.4 Block Diagram of Digital Gaussian Filter

while verilog starts at the 0 value. The Gaussian filter was synthesized for the Xilinx Virtex FPGA V800HQ240-4 using Program Manager 4.2i. The synthesized design uses 62 FlipFlops and 113 CLBs.

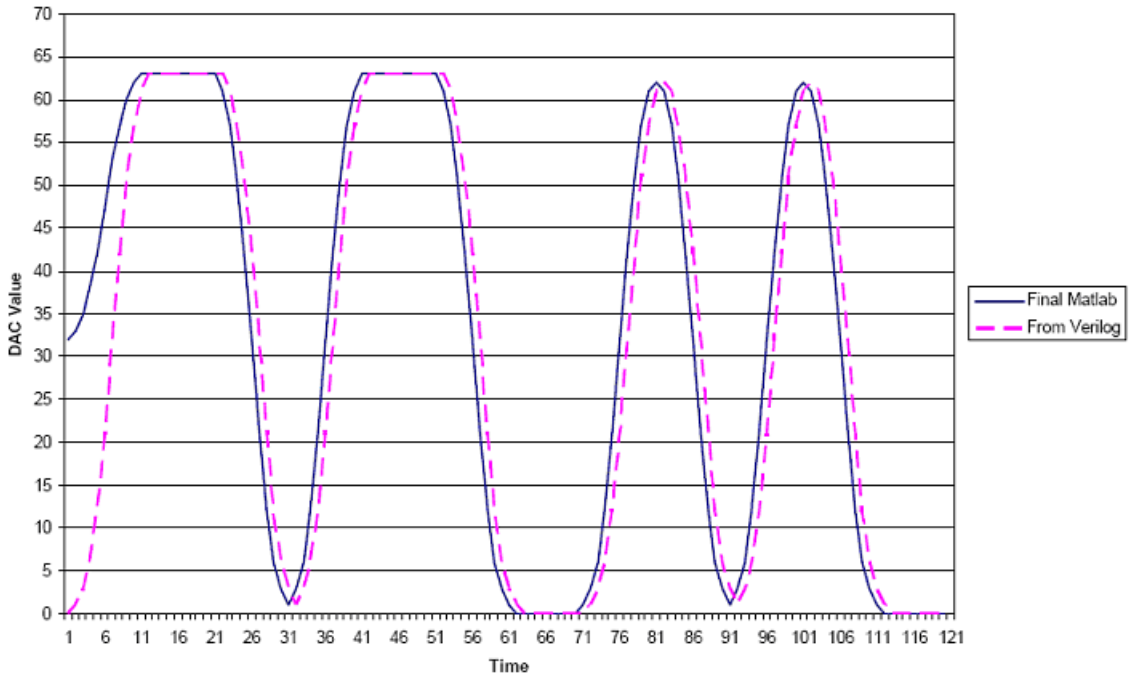


Figure 7.5 Comparison between Verilog and Matlab implementation of Gaussian Filter

7.4 Demodulation techniques

GFSK is basically a kind of frequency modulation technique, so various Frequency demodulation techniques could be used demodulate the GFSK signal. Various techniques used to demodulate the GFSK signal is briefly discussed here.

7.4.1 Frequency Discrimination

In this technique, frequency shift is translated into the amplitude change. Figure shows a circuit, which can act as the FM-to-AM converter (Frequency discriminator). This circuit multiplies the time-delayed signal with the original signal. The output of the frequency discriminator block with time delay τ depends on the phase difference between the original and time-delayed signals

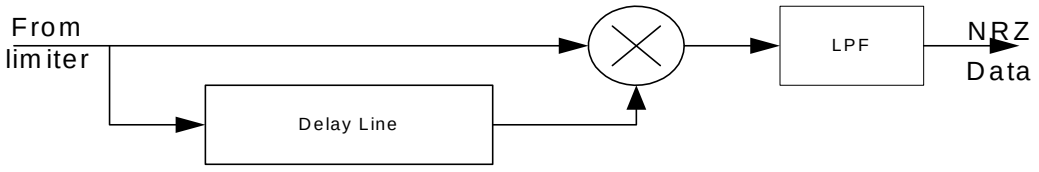


Figure 7.6 Frequency Discriminator

$$Vout = Cos(2\pi f + \theta) * \cos(2\pi f + \theta + \phi(\tau)) \quad \text{eq 7.8}$$

$$= \frac{1}{2} Cos(\phi(\tau)) + \cos(4\pi f + 2\theta + \phi(\tau)) \quad \text{eq 7.9}$$

If a low pass filter is used after the discriminator then the second term is assumed to be eliminated. So the output is solely dependant on τ. The time delay τ is chosen in such a manner Vout = 0 for f <= fc and Vout = 1 for f>fc , where fc is the center frequency.

7.4.2 Phase shift discrimination

The Phase shift discriminator is a better demodulation method than the FM discriminator as it utilizes only the phase of the signal. The figure shows a phase shift discriminator. First the incoming signal is down converted into a complex Baseband signal. The two path In-phase (I) and Quadrature (Q) path are low passed filtered to eliminate the high frequency products generated by mixing. Then using an arctan block phase is extracted. In order to retrieve the NRZ signal, the output of the arctan block has to be differentiated.

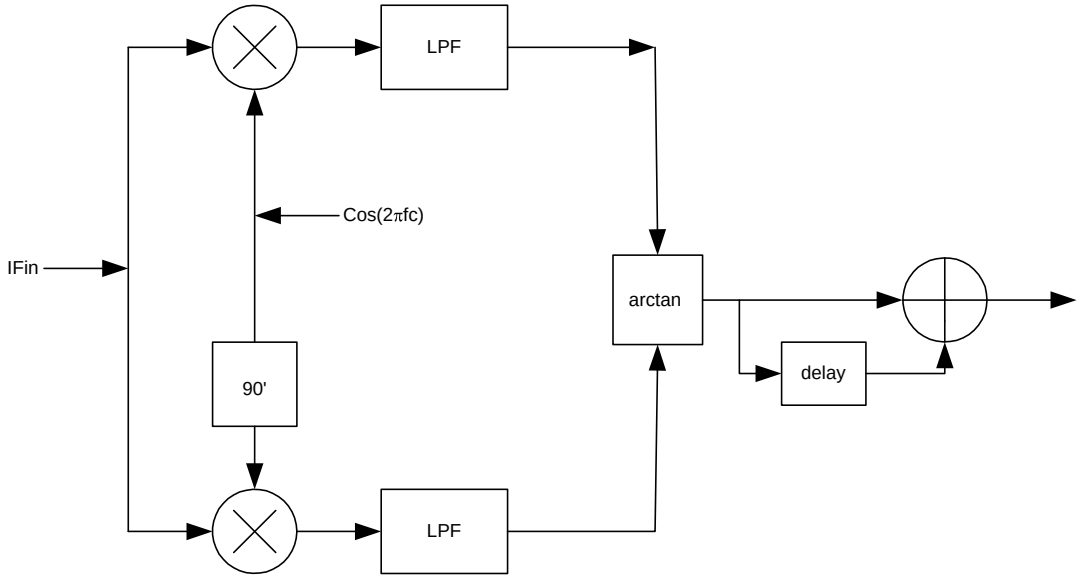


Figure 7.7 Phase Discriminator based gfsk demodulator

7.4.3 DLL based demodulator

A simple DLL based demodulator is presented by Sangjin [12]. The demodulator utilizes the fact that the period of the downconverted binary GFSK signal is continuously switched from $1/(f_{if} - \Delta f)$ to $1/(f_{if} + \Delta f)$, where f_{if} is the IF frequency and the Δf is the frequency deviation. And by comparing the period of the GFSK signal with the reference of $1/f_{if}$, the binary data could be recovered.

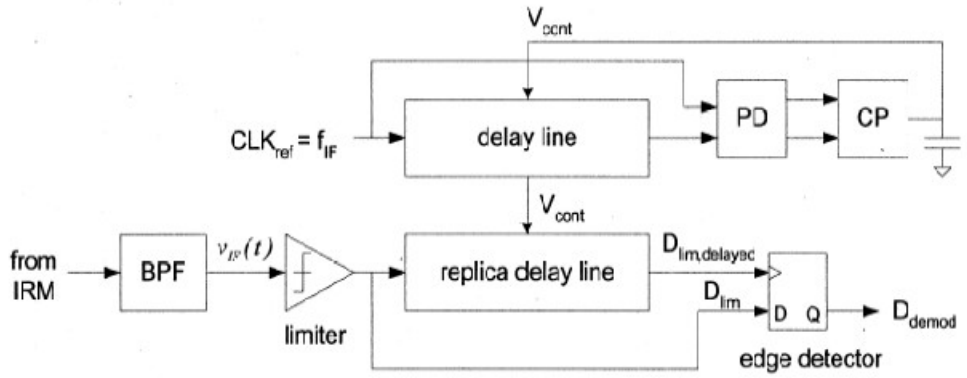


Figure 7.8 DLL based Demodulator

As shown in figure 7.8 the block diagram of the proposed DLL based demodulator. Since the DLL is locked to the reference clock of f_{if} , the replica delay line also provides the accurate delay of $1/ f_{if}$ which is used as the reference in the period comparison. The limiter output Dlim passes through the replica delay line to be delayed signal Dlim, delayed. Then, their rising edges are compared by an edge-detecting D flipflop. When the delay between the two signals is $1/ f_{if}$, the rising edge of Dlim,delayed leads or lags that of Dlim according to the received binary data. As a result, by detecting which rising edge comes first, the binary signal can be recovered from the GFSK modulated signal.

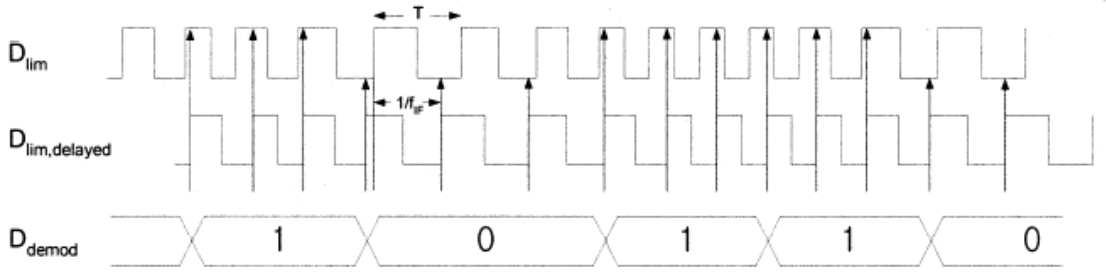


Figure 7.9 Demodulation waveforms

The downconverted GFSK signal at IF can be represented as

$$Vif(t) = A\cos(\int_{-\infty}^{t} 2\pi \times f(\tau)d\tau) \qquad \text{eq 7.10}$$

where f(τ)is the GFSK modulated frequency. From eq1, the time interval T between two successive rising edges of Dlim is determined as the time duration over which the integrated phase θ is equal to 2π.

$$\theta(t+T) - \theta(t) = 2\pi \qquad \text{eq 7.11}$$

Since the average frequency can be represented as the time interval T is equal to 1/favg.

$$favg = \frac{1}{T}\int f(\tau)d\tau \qquad \text{eq 7.12}$$

Thus the demodulator compares the 1/favg with 1/fif every m = 3 times per symbol period to recover the binary data, where m is the ratio of the IF frequency to the symbol rate.

The frequency discriminator has simple design but if there are any amplitude variation in the input signal then they get translated into the demodulated data degrading the BER. Phase discriminator on other hand would provide excellent BER but is more complex and requires more hardware. So DLL based frequency discrimination which both simple and provides a good BER performance was chosen for the transceiver design.

7.5 Summary

In this chapter, the open loop modulation method used to generate the GFSK modulation is discussed. A novel architecture for the gaussian filter occupying small area has been presented. Finally DLL based gfsk demodulation technique which gives BER of 0.1% for a SNR of 20 dB has been described.

8. Clock and Data Recovery

8.1 Introduction

The data stream received at the end of the demodulator is both asynchronous and noisy. Subsequent processing in higher layers of Bluetooth needs the synchronous data, so clock information needs to be extracted from this asynchronous data stream. The task of the clock extraction and data retiming is called “clock and data recovery” (CDR).

The data coming from the demodulator as shown in figure 8.1 is in Non Return to Zero (NRZ) format. This type of waveform is called NRZ to distinguish it from the Return to Zero (RZ) data, in which each bit consist of two section :- the first section assumes a value that represents the bit value, and the second section is always equal to a logical zero.

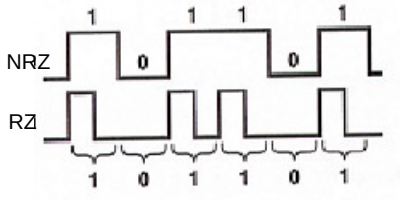
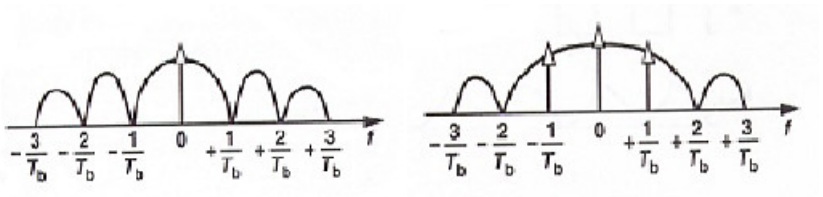


Figure 8.1 NRZ and RZ data format

As shown in figure 8.2a the spectrum of random NRZ data has a zero at the frequency equal to bit rate ($1/T_b$). So it doesn’t contain information of the clock to which it is suppose to lock to. In contrast to NRZ data, RZ waveform as shown in figure 8.2b exhibits a spectral line at a frequency equal to the bit rate, thereby simplifying the task of clock recovery [47]. So NRZ data needs to be converted into the RZ data so that it contains some information regarding the frequency to which it is suppose to lock to. A simple circuit that would allow doing that is shown in figure 8.3. Here data sequence and its delayed version are Xored, thereby producing a positive pulse of width ΔT on each data edge.



(a) (b)

Figure 8.2 Spectrum of (a) NRZ random data (b) RZ random data

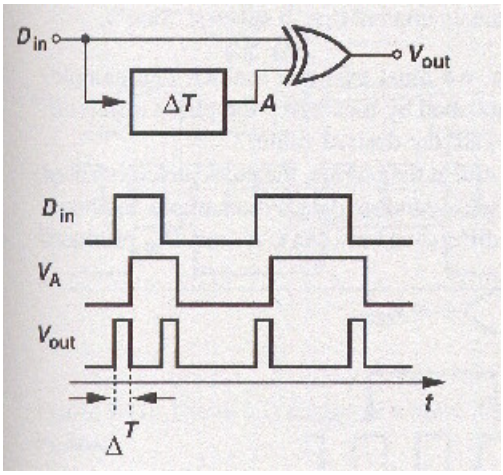


Figure 8.3 Edge detector Circuit

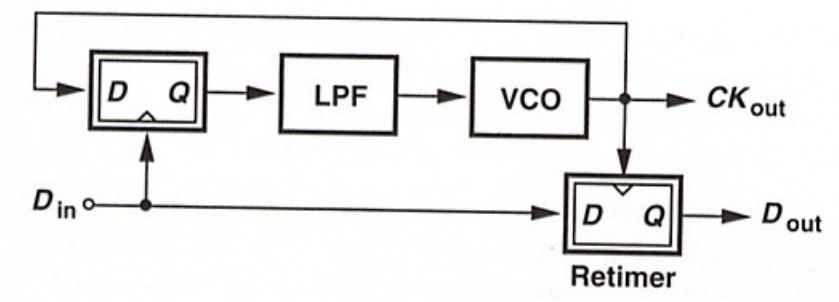


Figure 8.4 Block Diagram of Clock and Data Recovery Circuit

Above figure shows the top level block diagram of the clock and data recovery circuit.[47] Here to generate the clock signal, a VCO (Voltage Controlled Oscillator) is used and to define its frequency and phase, we phase-lock the VCO to the input data. Also to retime the data, we add another DFF that is clocked by the VCO output. The recovered clock Ckout drives input of phase detector and clock input of the retimer.

This circuit operates as follows. Upon turn-on the DFF multiplies the edge-detected data by the VCO output, generating a beat that drives the VCO frequency towards the input rate. But if the initial difference between the VCO frequency and the data rate is sufficiently small, then the loop locks, establishing a well-defined phase relationship between Din and Ckout.

8.2 Implementation

An all-digital PLL was created whose architecture is similar to 74HC/HCT297 was used in designed Clock And Data Recovery Circuit [45,46]. The block diagram of this CDR circuit is shown in figure 8.5.

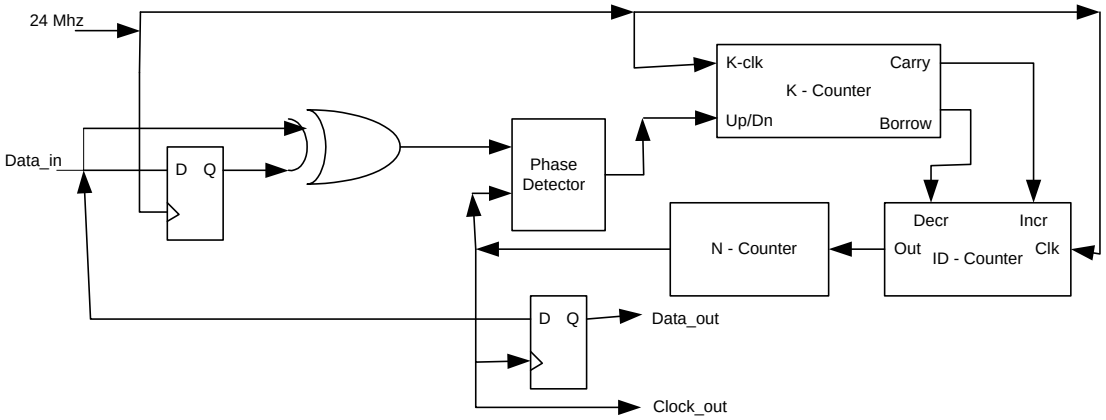


Figure 8.5 Implementation of CDR Circuit

Here edges of in-coming data sequence are extracted using the Xor and D flip-flop operating at 24 Mhz. This edge information is then feed to the All Digital PLL to extract the clock information. The basic operation of this All Digital PLL could be understood from the bellow figure.

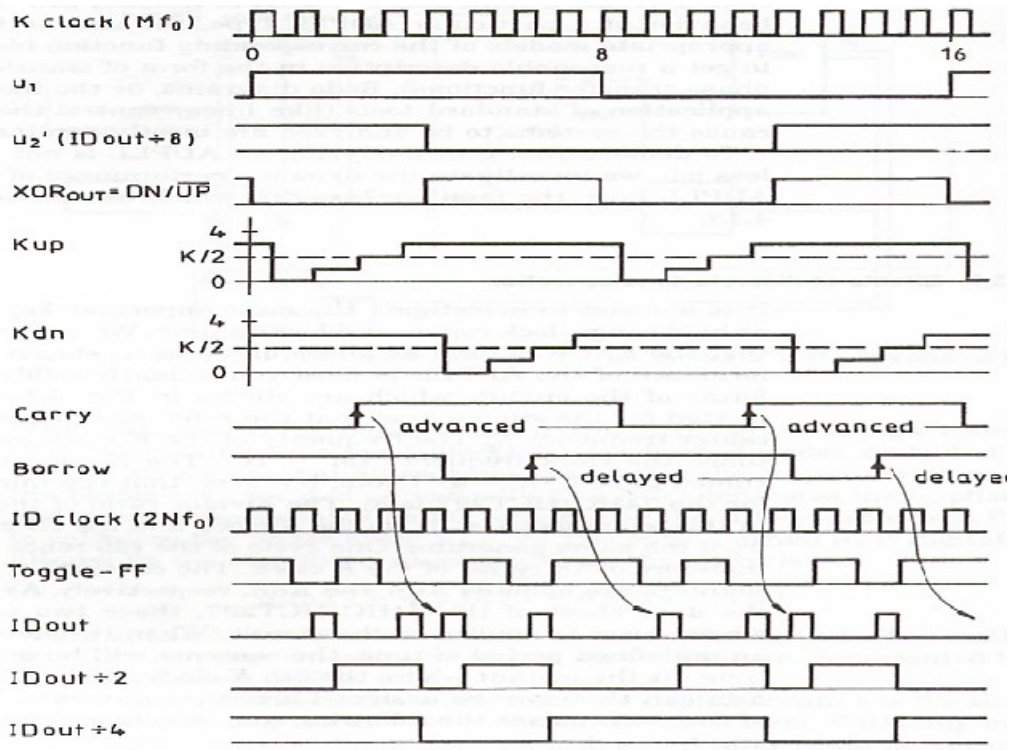


Figure 8.6 Operation of All Digital PLL

Here a simple xor gate is used as the phase detector which generates up /down signal. These up/down is filtered through the K-counter which generates carry or borrow signal once every K cycles. Based on the carry/ borrow signal ID counter generates an extra or swallows a pulse. The output of ID counter is divided to get the clock_out.

8.3 Summary

A CDR for 1 Mbps data rate was designed in verilog HDL. The circuit uses the 24Mhz clock as input and various counter are configured as K=6, N= 12 and M=24; so as give the settling time of 2μs and hold frequency of ± 166khz.

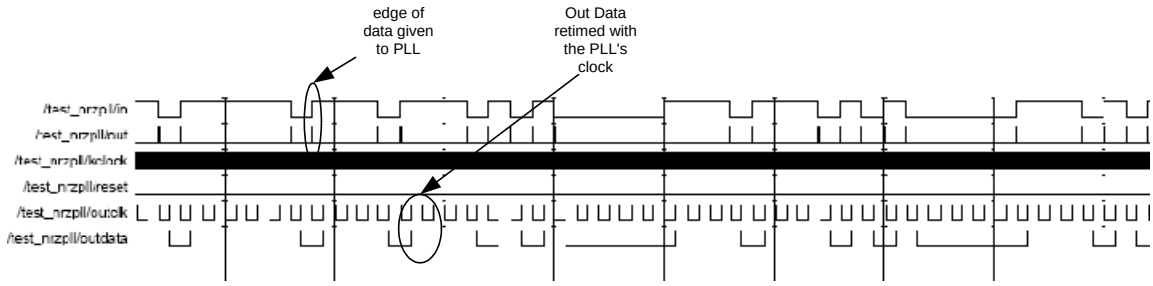


Figure 8.7 Simulation of verilog module of CDR

9. Sigma Delta DAC

9.1 Introduction

Over-sampled (sigma delta) A/D and D/A are gaining popularity in high-resolution medium to low speed application for two main reasons.

1. Over-sampled converters relax the requirements placed on the analog circuitry at the expense of more complicated digital circuitry. This trade-off becomes more desirable in submicron technologies as with reduced power supply voltages like 1.5V, the complicated high-speed digital circuitry is easier to design in less area. But designing a high-resolution analog circuitry is complicated by low power supply voltage and poor transistor characteristics.
2. They simplify the requirements placed on the analog anti-aliasing filters for A/D converters and smoothing filters for D/A.

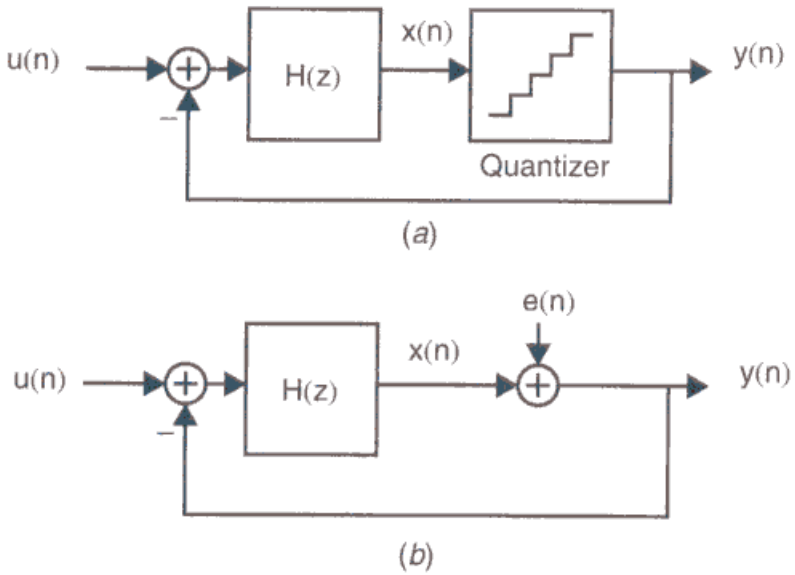


Figure 9.1 (a) First order Sigma Delta Modulator (b)Linear model of the modulator

A general noise shaped delta-sigma (ΔΣ) modulator and its linear model are shown in figure.

Treating the linear model shown in Figure b as having two independent inputs , the signal transfer function (STF) and Noise Transfer Function (NTF) can be derived as bellow

$$STF(z) = \frac{Y(z)}{U(Z)} = \frac{H(z)}{1 + H(z)} \qquad \text{eq 9.1}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \qquad \text{eq 9.2}$$

In frequency domain, the output signal as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function is given as bellow.

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \qquad \text{eq 9.3}$$

To noise shape the quantization noise in a useful manner, we choose H(z) such that its magnitude is large from 0 to fc (ie, over the frequency band of interest). With such a choice, the signal transfer function, STF(z) will approximately unity over the frequency band of interest. Furthermore, the noise transfer function, NTF(z) will approximate zero over the same band. Thus, the quantization noise is reduced over the frequency band of interest while the signal itself is largely unaffected. The high frequency noise is not reduced by the feedback, as there is little loop gain at high frequencies. However, additional post filtering can remove the out of band quantization noise with very little effect on the desired signal.

9.2 Implementation and design flow

To convert the 8 bit digital output of the Gaussian filter to analog signal which could be fed to the VCO to generate direct gfsk modulation, a sigma delta DAC with SNR (signal to noise ratio) equal to 64dB was designed. The design flow used to design this sigma delta dac is shown in figure 9.2.

Various matlab scripts (synthesizeNTF, realizeNTF, SNR, etc) were written to help to design and analyze the sigma delta modulator design [49]. Then simulink models were created and simulate to calculate the actual SNR. When required SNR was achieved a verilog HDL code was written for that modulator. A small program was written which could capture the input signal values from matlab into a file. This file is then read by the verilog testbench, which simulates verilog hdl sigma delta module and store its output in another file which matlab could read and plot the output of verilog code and its side-by-side for comparison as shown in figure 9.3.

9.3 Summary

A simple design for 3rd order Sigma delta D/A converter is presented in this chapter. The designed sigma delta D/A converter has a dynamic range equivalent to 8 bits.

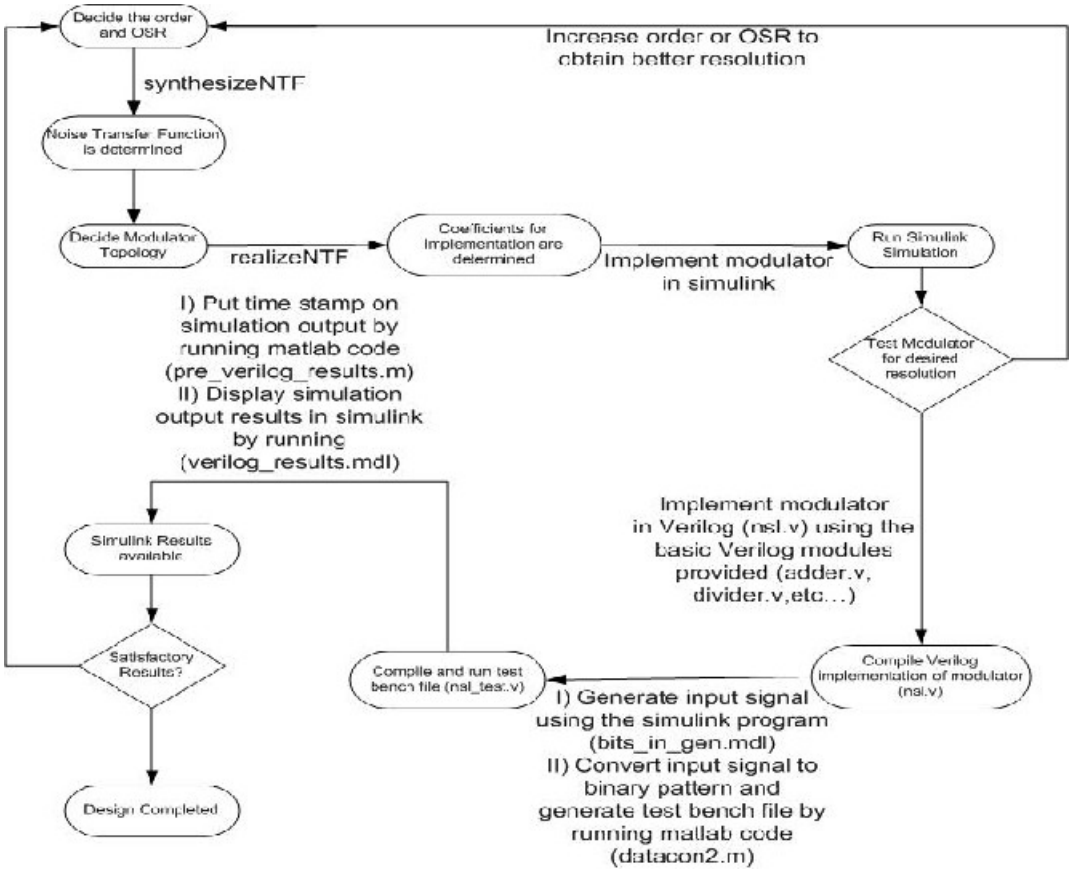


Figure 9.3 Design flow of Sigma Delta D/A converter

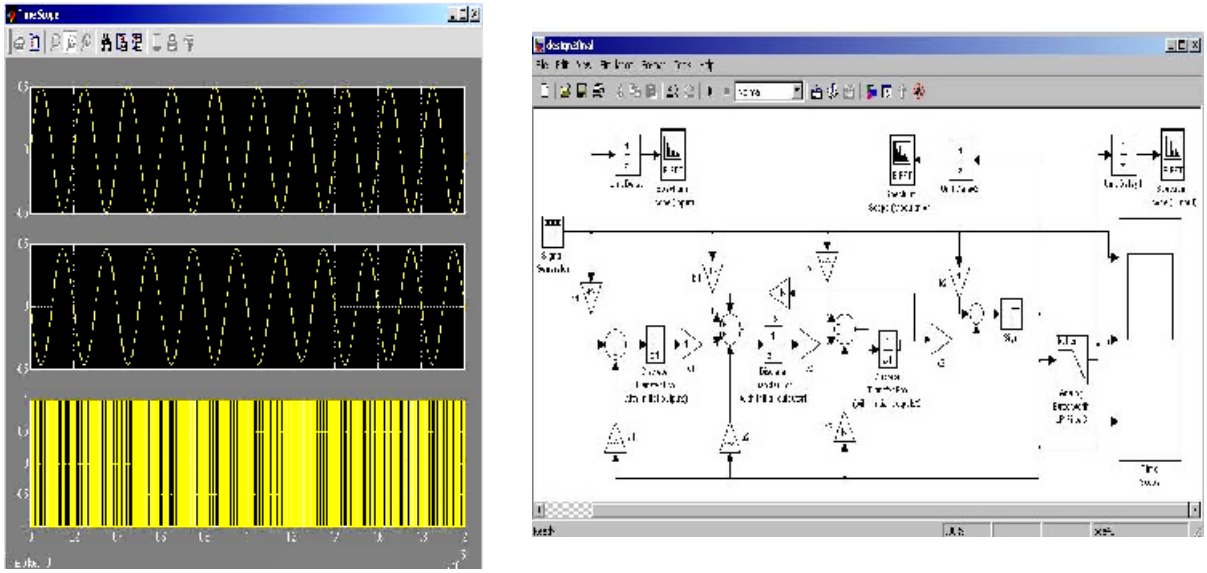


Figure 9.3 Side-by-side comparison of Verilog and Matlab output

10. Sigma delta Frequency Synthesizer

10.1 Introduction

PLL helps in keeping the VLSI circuit orderly. A Phase-Locked Loop is a feedback system combining a voltage-controlled oscillator and a phase comparator so connected that the oscillator frequency (or phase) accurately tracks that of an applied frequency- or phase-modulated signal. A French engineer, De Bellescize, implemented the first phase-locked loops in the early 1930s. However, they only found broad acceptance in the marketplace when integrated PLLs became available as relatively low-cost components in the mid-1960s. They have wide range of application like frequency synthesizer, frequency modulator/demodulator, filter tuning, clock synthesis, clock retiming, clock & data recovery, etc.

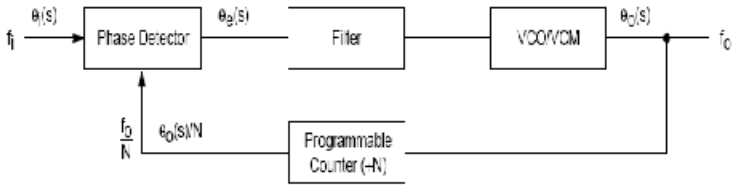


Figure 10.1 Phase Locked Loop

Traditionally, there are two major ways of generating frequencies: direct and indirect. In direct approach, the sine wave is generated digitally by storing the sine wave in read-only memory (ROM) followed by the D/A conversion. Even though this approach is simple and would generate sine wave with good spectral purity, it needs a high speed D/A, which becomes the bottleneck. While in indirect method high frequencies are generated with VCO (voltage controlled oscillator). Since the noise property and frequency stability of such VCO is usually poor, it is typically put in a feedback loop to enhance these properties. Since the loop tracks the phase of the VCO, it is called a Phase locked loop (PLL) and so this indirect approach is called PLL based frequency synthesizer. Based on types of divider in PLL frequency synthesizer, they are classified as

1. Integer-N Synthesizer

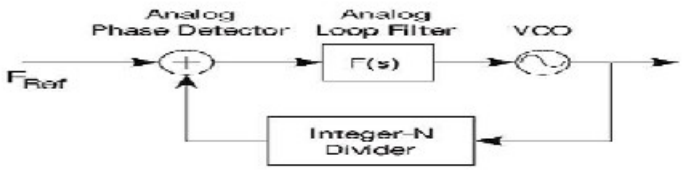


Figure 10.2 Interger-N Synthesizer

Integer-N synthesizer give frequency which are in integer multiple of reference frequency. As shown in above figure, to generate the desired VCO frequency, Integer-N divider divides the VCO frequency by a value N. Although this scheme has simple design it suffers from relatively large phase noise as it increases by 20log(N)[47]. They also have long settling time as loop filter's bandwidth is limited by F_{ref}.

2. **Fractional-N Synthesizer**

In Fractional-N Synthesizer, the output frequency can vary by a fraction of the input frequency. As shown in figure, if prescaler divides by N for A output pulses of VCO and by N+1 for B output pulses, then the equivalent divide ratio is equal to :-

$$N.f = (A+B)/[A/N + B/(N+1)] \qquad \text{eq 10.1}$$

where N = Integer part of the modulus

f = fractional part of the modulus

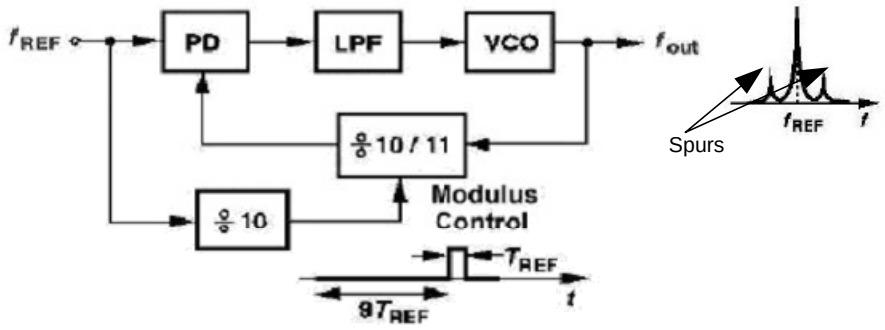


Figure 10.3 Fractional-N Synthesizer

As an example, if f_{ref} = 1Mhz and N= 10 and if we assume the prescaler divides by 10 for 9 reference cycle. The total number of output pulses is therefore equal to 9x10+11=101, where reference produce 10 pulses. In other words, the divide ratio is equal to 10.1 and f_{out} = 10.1 Mhz. Now due larger reference frequency, it is possible to design PLL with bigger loop bandwidth, which results in faster settling time. But now as the phase detector produces progressively wider pulses, creating a ramp waveform at the output of the LPF causing Spurs to appear in frequency spectrum as shown in figure. These fractional spurs could be eliminated if choice of modulus is randomized in such a way that the average division factor is still same. ΣΔ modulator can easily achieve this randomization.

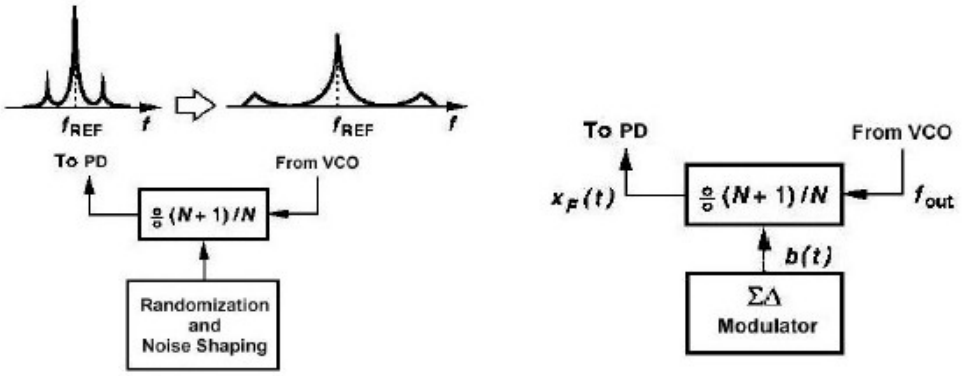


Figure 10.4 A Method for reducing the fractional spurs

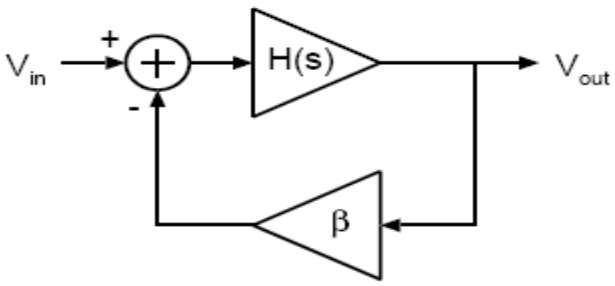
According to the Bluetooth specification, the frequency synthesizer should be able to generate frequency from 2.402GHz to 2.48GHz with the frequency tolerance of ±75Khz. Also as frequency hop occurs after ever 625μs, so the worst case settling time should be (3125-2871) = 254μs. Also as direct modulation is being done, frequency synthesizer should be capable of generating GFSK modulation with modulation index of 0.28-0.35, i.e. it should be capable of generating a frequency deviation of 140Khz-175Khz.

10.2 Implementation

A Phase lock loop is made up of many components like VCO, Divider, Phase detector, Charge pump and a filter. Design of Each of these components is discussed here.

10.2.1 Voltage Controlled Amplifier (VCO)

Voltage controlled amplifier is one of the key building blocks of radio frequency transceiver system. They are used for carrier frequency synthesis for up and down convert the signal. Figure shows the general model of negative feedback system, which is acting as an oscillator.



$$\frac{Vout}{Vin}(s) = \frac{H(s)}{1+\beta H(s)}$$

If this negative feedback circuit has a loop gain that satisfies two conditions :-

$$|\beta H(s)| \geq 1$$

$$\angle \beta H(s) = -180'$$

then the circuit may oscillate. These necessary but not sufficient conditions are called Barkhausen Criteria. For CMOS oscillators two common methods to realize such a negative feedback system that fulfills the Barkhausen Criteria are

1. Ring Oscillator

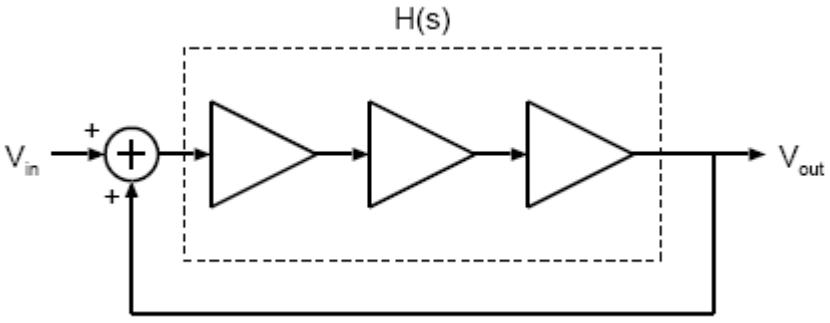


Figure 10.5 Ring Oscillator

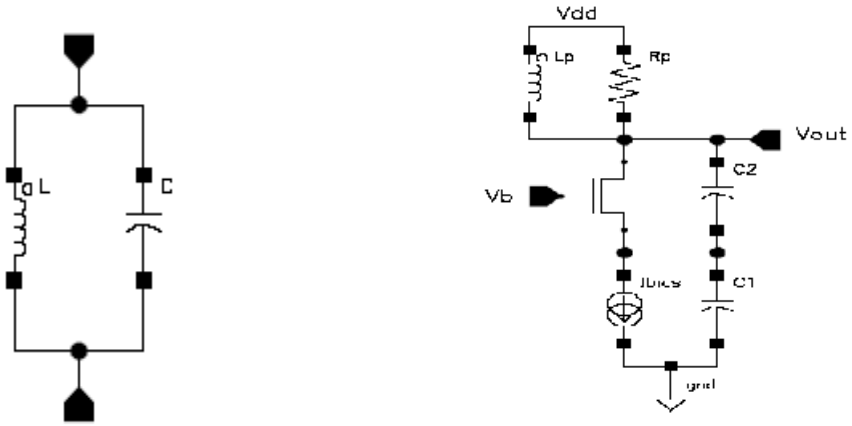
A ring oscillator consist of at least three gain stages each of them introducing an additional pole and therefore a phase shift of 90' in the closed loop transfer function. It is therefore possible that this system has $|\beta H(s)| \geq 1$ and $\angle \beta H(s) = -180'$, thus fulfilling the barkhausen criteria. The major advantage of ring oscillator is that they generate oscillations without any passive elements like capacitors and inductors.

But there is no filtering action, which would shape the phase noise of the output signal. Therefore ring oscillators generally show a very poor phase noise performance compare to LC oscillators [24].

2. LC Oscillator

An LC oscillator consist of parallel combination of an inductor and a capacitor plus an active circuit, which compensates for the losses in the passive elements. The parallel combination of inductor L and the capacitor C forms the oscillator tank as shown in figure. The oscillator tank resonates at the frequency

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{eq 10.2}$$



(a) (b)

Figure 10.6 a) LC oscillator (b) Colpitts' Oscillator

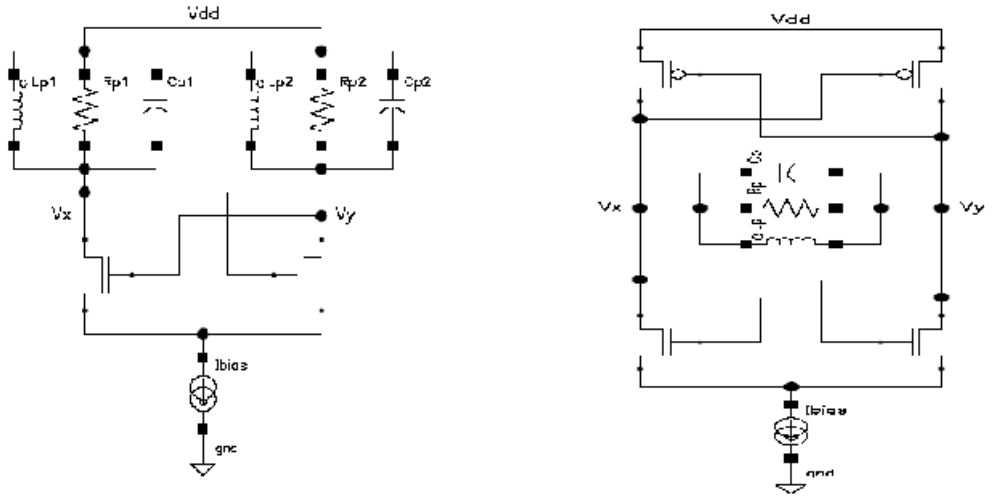
LC oscillators can be created with one, two or four transistors, which provide a sufficient gain for oscillation. Figure 10.6b shows the Colpitts oscillator structure, which uses a single transistor to generate oscillation. Analysis of this circuit reveals that the single transistor should have a transconductance (g_m)

$$g_m \geq \frac{4}{R_p} \qquad \text{eq 10.3}$$

to provide the sufficient oscillations. But for cross coupled Nmos only oscillator structures shown in figure 10.7a requires only a transconductance of

$$g_m \geq \frac{1}{R_p} \qquad \text{eq 10.4}$$

Thus cross-coupled structure could achieve same oscillations as Colpitts while occupying smaller area. Thus cross-coupled structures are preferred to the Colpitts in integrated oscillators.



(a) (b)

Figure 10.7 (a) Nmos only LC oscillator (b) Nmos-Pmos cross coupled oscillator structure

The Nmos-Pmos cross coupled oscillator structure shown in figure 10.7b adds a differential Pmos pair on the top of a Nmos only cross-coupled oscillator. This topology has several advantage over the Nmos only counterpart like

1. For the same bias current, the Nmos-Pmos structure attains a peak differential output amplitude Vx-Vy twice as high as the Nmos only structure.

2. For a given bias current, the Nmos-Pmos structure attains a negative resistance of $\frac{-2}{g_{mn}} + \frac{-2}{g_{mp}}$. While for the same bias current, the Nmos only structure attain a negative resistance of $\frac{-2}{g_{mn}}$. With the addition of Pmos transistors, it therefore becomes possible to compensate for the loss in the LC tank with a lower bias current than in Nmos only structure.

3. By sizing Pmos and Nmos transistors so that $g_{mn} = g_{mp}$ makes it possible to attain a more symmetric oscillator waveform for Vx andVy than in Nmos only structure. This improves the rise time and fall time

symmetry, which reduces the up-conversion of the transistor 1/Δf noise. Therefore, Nmos-Pmos structures attain a smaller $1/\Delta f^3$ noise corner in phase noise characteristics than Nmos only structures does.

Due to all these advantages, Nmos-Pmos topology was chosen for the VCO design. To have the frequency tunnability a pair of varactors were added to the circuit. Additional pair of small varactors form with Nmos transistors was added, so that open loop frequency modulation can be achieved. The circuit was simulated in ADS and cadence's SpectreRF simulator and figure 10.8 shows the various Phase noise of the oscillator. Figure 10.9 shows the voltage tunnability of the VCO.

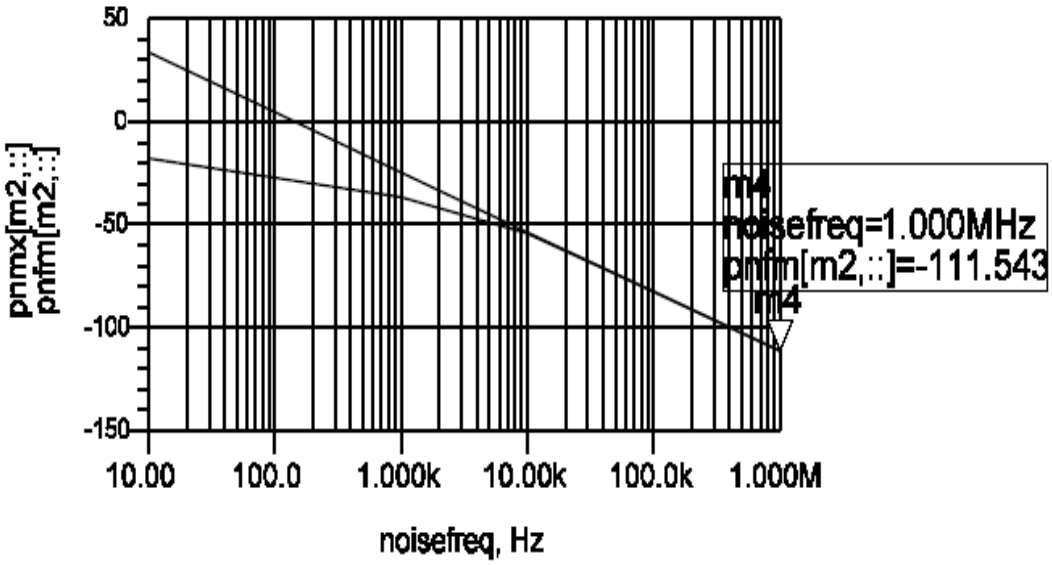


Figure 10.8 Phase noise of the Oscillator

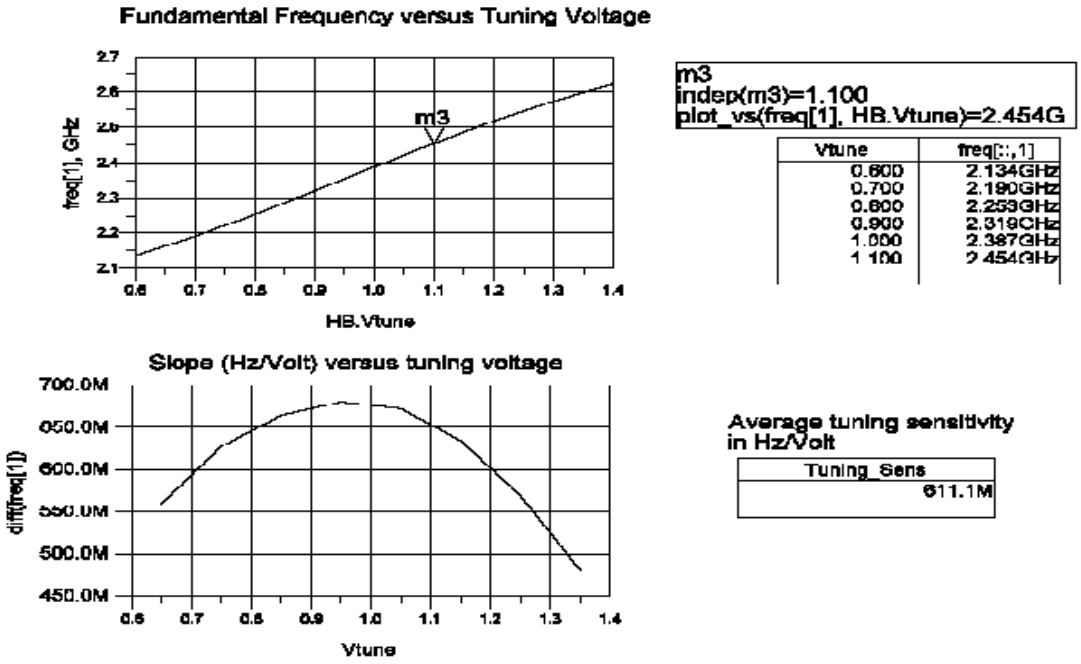


Figure 10.9 Voltage tunnability of VCO

10.2.2 Dividers

Frequency dividers also known as prescaler are used to convert the high frequency output of the VCO to something equivalent to reference frequency which is normally at very low frequency. A dual modulus N/M divider, or prescaler, performs frequency division to produce an output with a cycle time that equals either N or M cycles to its input. Most modern frequency synthesizer have an architecture that consists of a pulse swallowing state machine at the input followed by an asynchronous ripple counter. The Advantage of this topology is that only a small section of the overall divider operates at the high frequency of the input; the stages following operates at progressively lower frequency.

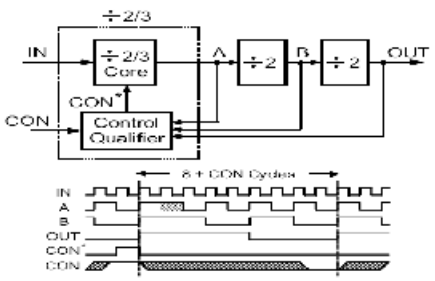


Figure 10.10 8/9 dual modulus prescaler

The dual-modulus approach can be extended to realize multi-modulus prescaler that are capable of frequency division over a large range. To do so, the asynchronous divides by 2 sections of the dual modulus divider are replaced with divide by 2/3 dividers. This design increases the range of divide values to include all integers between 2^k and 2^{k+1}-1, where k is the number of divide stages within prescaler. As this method uses asynchronous counting method, the speed and power dissipation remains comparable to the dual modulus approach.

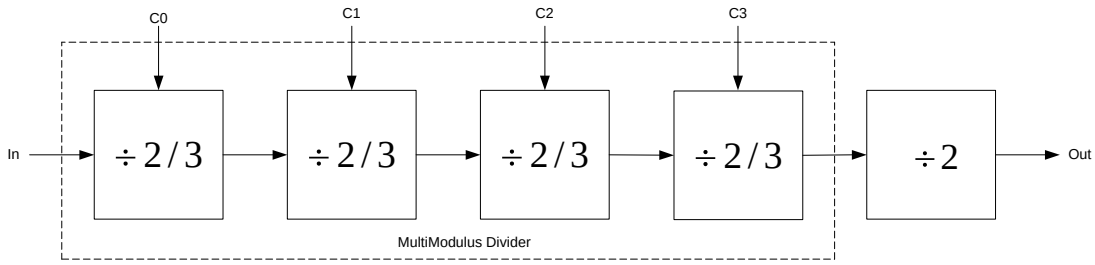


Figure 10.11 MultiModulus divider

Above figure shows the architecture of the divider used in the frequency synthesizer. It consist of 4 2/3 divider configured as multimodulus divider followed by a divide by 2 stage. The multimodulus divider is capable of providing the division ratio of 16,17,18,….31. Thus this divider would provide the total division from 32 to 62. Now as reference frequency is kept at 48Mhz and the frequency synthesizer needs to sweep the frequency from 2.4Ghz to 2.5Ghz, thus a divider ratio of [50,52] is needed which could be achieved through above divider.

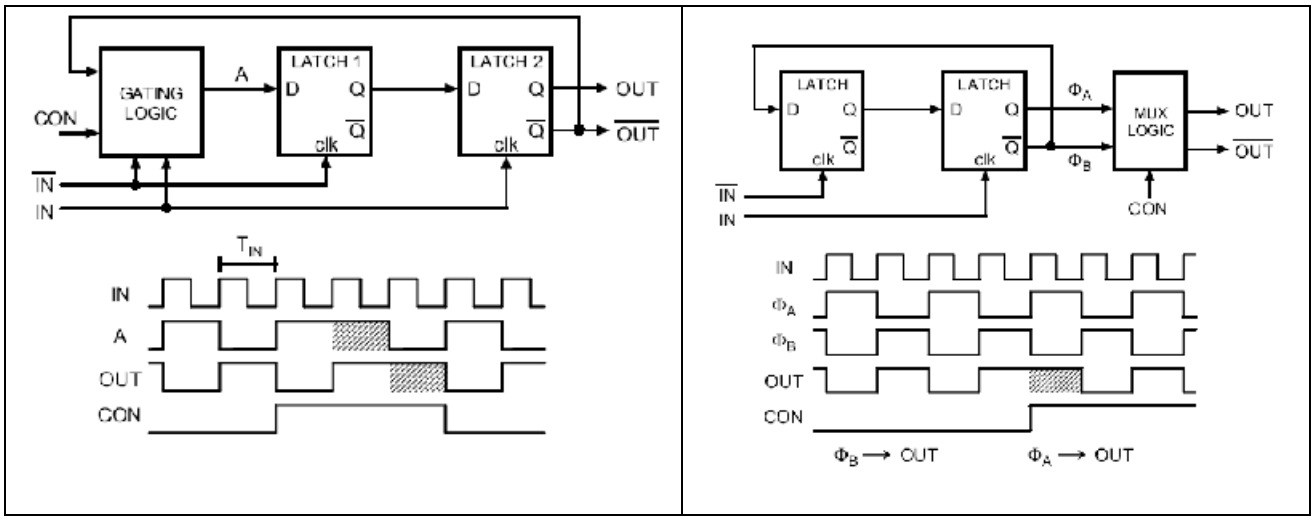


Figure 10.12 Two ways of designing divide by 2/3 circuit

To create a divide by 2/3 circuit, a common approach is to augment the Johnson counter to swallow cycles by gating the feedback signal into one of its latches. Above figure shows a divide by 2/3 circuit, when CON signal is equal to 1, divide by 3 occurs. The addition of gating circuit at the front limits the speed of operation of the divider and also increases the power consumption. Alternatively divide by 2/3 operations can be achieved by phase select as shown in figure. Here phase selection is done by a Mux operates at the half frequency of the input. Thus this circuit is less power hungry and so is used in the multimodulus divider operation.

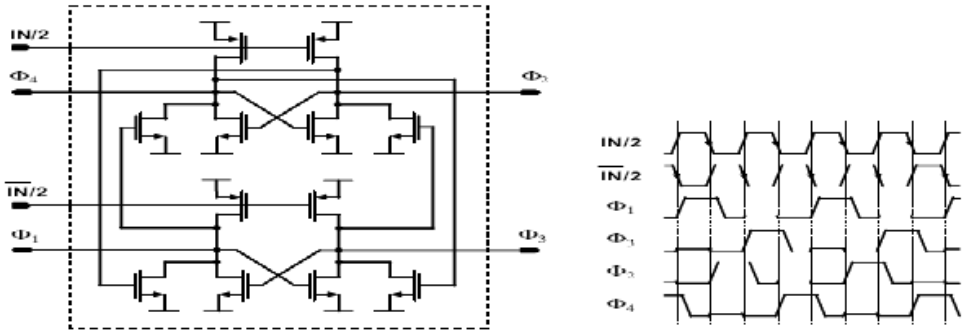


Figure 10.13 Divide by 2 Circuit

Above figure show the circuit of a high speed, four phases, divide by 2 topology that is capable of operating at high speed. It structure is essentially a Johnson counter that achieves high speed by avoiding the stacking of NMOS or PMOS transistors. The latch operates by using PMOS devices to drive current into its output nodes according to a clock signal, and NMOS selectively discharges the nodes according to the signals supplied by the other latch.

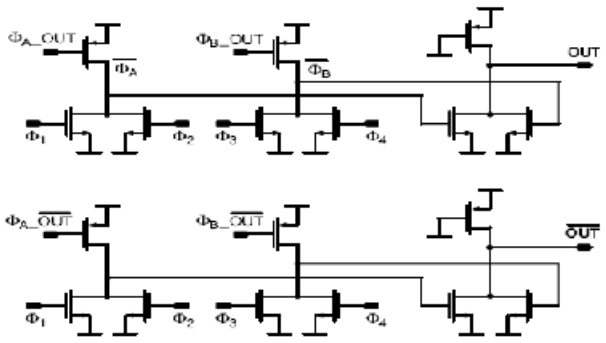


Figure 10.14 High Speed Mux design

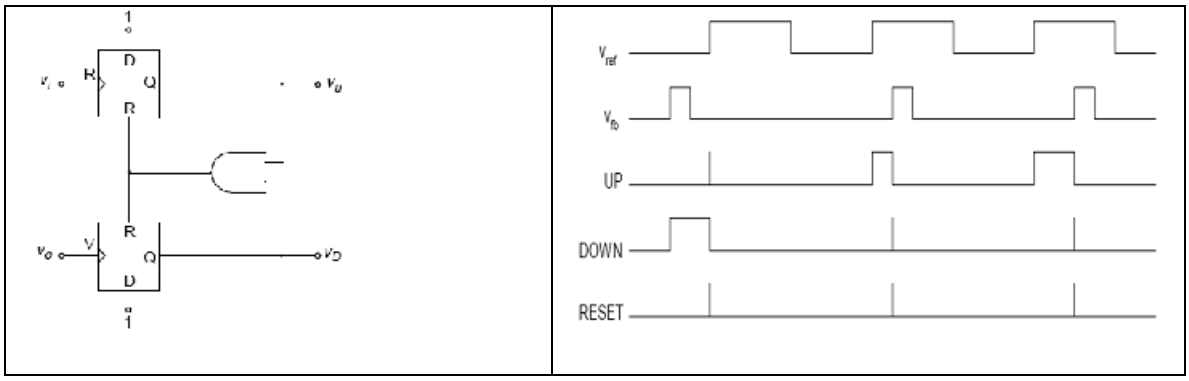
The four phases generated by the divide by 2 circuit are combined with an OR operation as shown in above figure to produce two complementary phases, ϕ_A and ϕ_B. These phases are gated to the output signals, OUT and OUTbar, using PMOS devices that are controlled by four different control signals as shown in above figure.

10.2.3 Sigma delta modulator

A third order 16 bit SD modulator similar to the one used in SD DAC is used here in frequency synthesizer. The modulator has a single bit output which is used to select the division ratio of 50 or 52. The sigma delta modulator help in getting rid of the fractional spurs present which are normally present in Fractional N frequency synthesizer. It also helps to improve the phase noise characteristics of the SD modulator by reducing the phase noise associated with the charge pump and the folding of phase noise due to PLL nonlinearities.

10.2.4 Phase Detector

Phase detector (PD) senses the phase difference between the reference frequency and divided VCO output and produces a dc value, which is proportional to their phase difference. The accuracy of the phase detection determines the spurious tone magnitude. Existing phase detectors include Gilbert multiplier, double-balanced multiplier, triangular phase detector, etc. In this application, a tri-state phase/frequency detector is chosen for its operation with the charge pump. Figure shows the state and logical block diagram of a tri-state phase/frequency detector [45]. With three states, this phase detector can detect both phase and frequency. Assuming the flip-flops are triggered on the rising edge, will cause the (UP) waveform to rise and will cause the (DN) waveform to rise. When both and are high, the *AND* gate resets the flip-flop and both and are brought back to zero immediately.



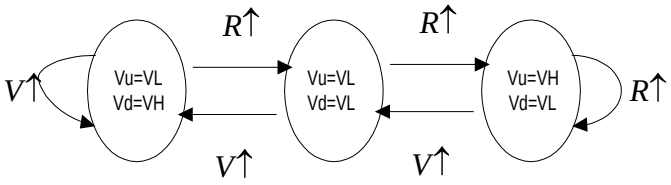


Figure 10.15 Phase Frequency Detector (PFD)

This phase detector generates two pulses whose pulse width difference is ideally equal to the phase difference of the input signals. Depending on the time delay of the reset path, the shorter pulse might be a small spike due to the finite rise and fall time in logic gates. In order to achieve a better matching between UP/DN pulses, extra delays are inserted in the reset path to increase both pulses' widths by the same amount. The upper limit for the extra-added delay in the reset path is the noise performance. These two signals are used in the charge pump to convert the phase difference information to an electrical signal.

10.2.5 Charge pump

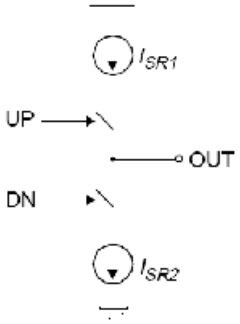


Figure 10.16 Charge Pump

Above figure shows the conceptual diagram for a charge pump. The UP/DN signals generated by the phase detector are used to time-multiplex the currents from the current sources, I_{SR1} and I_{SR2}, into the output node.

Assuming that $I_{SR1} = I_{SR2}$, and the UP/DN pulse shapes and switches are ideal, the pulse width difference between the UP and DN signals is proportional to the charges deposited and withdrawn at the output node. For example, if inputs to the phase detector are perfectly in-phase and the UP/DN signals are identical; the current measured at the output node would be ideally zero. On the other hand, if the inputs to the phase detector are not in-phase, the average current measured at the output is $\frac{I_{SS}}{2\pi}\theta_e$, where θ_e is the phase difference between the two inputs to the phase detector. Therefore, the combined transfer function for the phase detector and charge pump is

$$K_{pd\_cp} = \frac{I_{SS}}{2\pi}$$

In standard frequency synthesizer with tri-state operation, the current consumption of the charge pump is lower than few hundred μA depending upon the clock frequency and the turn on time of the PFD.

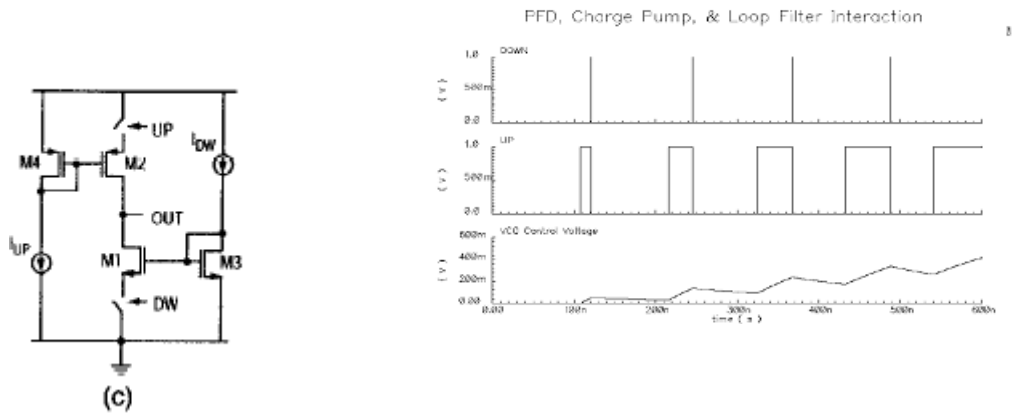


Figure 10.17 Charge pump circuit design

Above figure shows the schematic of the charge pump used in the frequency synthesizer [51]. The advantage of this schematic is that the current mirror transistors M1-M2 always remain in saturation all the time. As a result, a low bias current can be used with high output current, which lowers the power consumption. Also this architecture gives faster switching time than the gate switching since the switch is connected to single transistor with lower parasitic capacitance.

10.2.6 Filter

The function of a loop filter is to remove the high frequency components in the charge pump output and produce a control voltage to adjust input voltage of the Varicap of VCO.

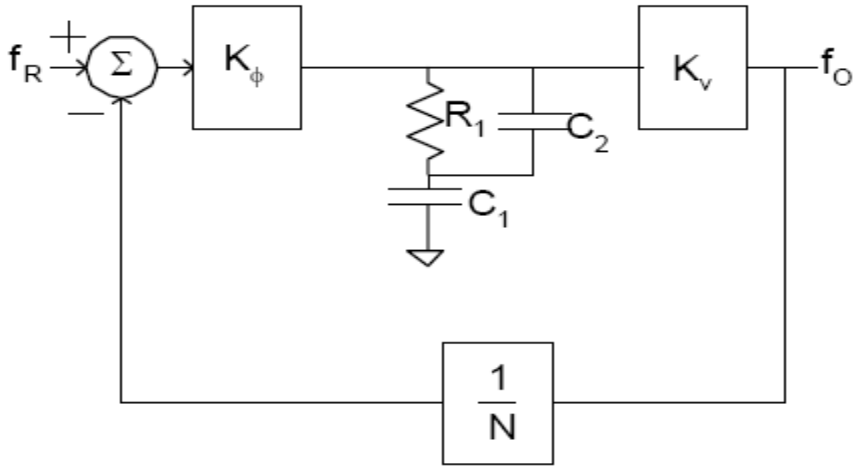


Figure 10.19 Third order PLL

The transfer function of this Phase lock loop can be given by

$$H(s) = K_{\phi} \frac{R_1(C_1 + C_2)s + 1}{C_1 s(R_1 C_2 s + 1)} \frac{K_v}{s} \frac{1}{N}$$

where

Kϕ=2π x 100μA (charge pump current)

Kv=2π x 800 Rad-Mhz/V (VCO sensitivity)

N = 50 (Divider ratio)

By keeping the Phase Margin 45’ and unity gain frequency of 50Khz, the values of the components of the filter were calculated as

R1= 26 Ω

C1 = 256 nF

C2 = 51 nF

These values are too large to be fabricated, so are place outside the chip. To do this only single pin would be required. With this filter a settling time of 65μs is achieved.

The frequency synthesizer with sigma delta modulator was simulated in the ADS simulator. Figure 10.19 shows the response of PLL to frequency step. Figure 10.18 shows the simulation result of system simulation of sigma delta pll and how fractional spurs are eliminated by the sigma delta modulator.

10.3 Summary

A fractional-N based frequency synthesizer is presented in this chapter. Sigma delta pll achieves a settling time period of 65μs and a VCO having a phase noise of –111dBc/Hz @ 1Mhz have been designed of this Bluetooth transceiver.

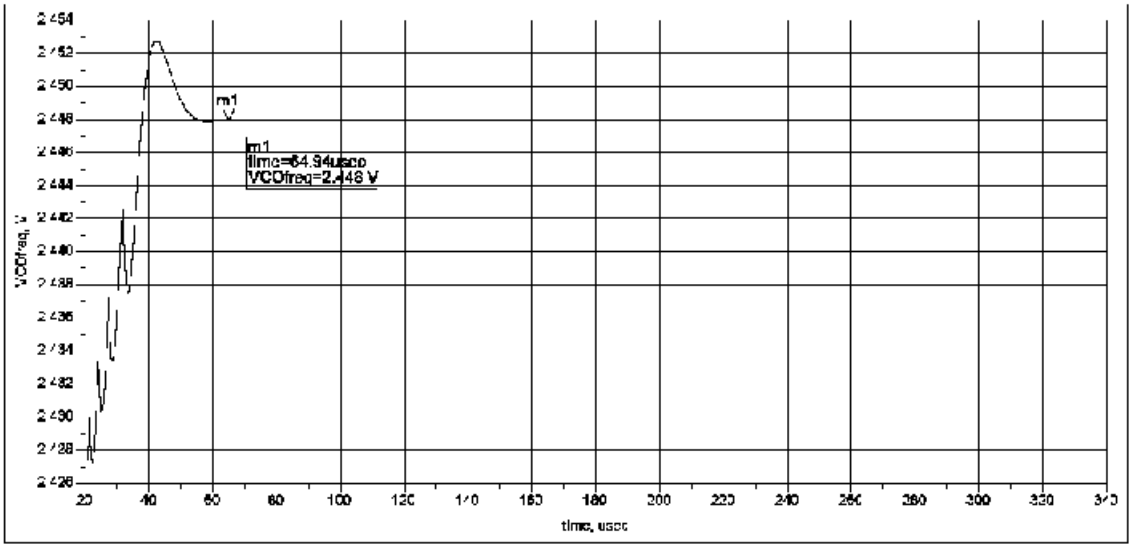


Figure 10.19 Settling time of PLL

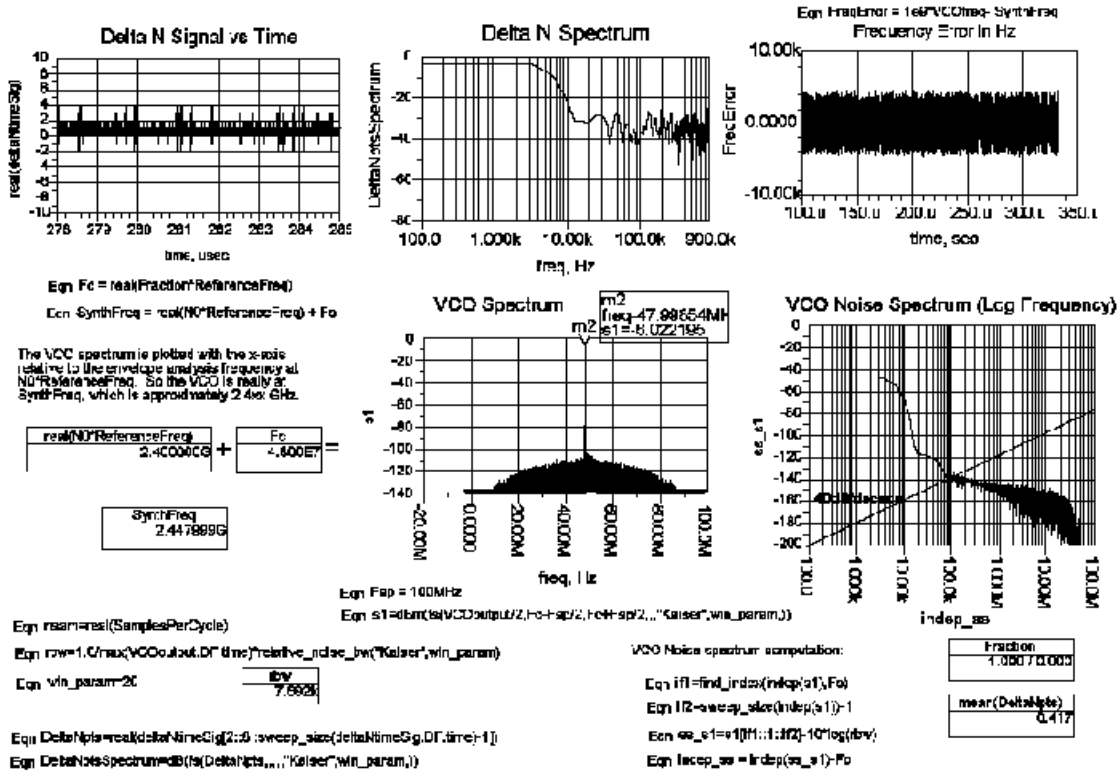


Figure 10.20 Simulation result of Sigma delta PLL

11. Conclusion

A surge in the demand for the wireless voice and data communication has driven the recent efforts to substantially increase the integration level of RF transceivers for cost and form-factor reasons. One way of doing this by implementing all the RF functions in the low cost standard CMOS technology, so that the RF and baseband sections can be combined into a single chip. The designed Bluetooth transceiver is a monolithic CMOS transceiver and doesn't need external matching network. The designed receiver circuit has input sensitivity of –80 dBm @ BER = 10-3 and Transmitter is capable of transmitting with a power of 4 dBm. The key features of various blocks of transceiver are given in table bellow.

Table 11.1 Key Features of Transceiver Design

Component	Feature	Value
Switch	Insertion Loss	-0.837 dB
	Isolation	-36.7 dB
	Noise Figure	1.2 dB
	1 dB compression	12.37 dBm
LNA	Gain	12.57 dB
	Noise Figure	2.3 dB
	IIP3	+4.04 dBm
	Input VSWR	1.41
	Output VSWR	1.8
Mixer	Conversion Gain	7.4 dB
	Noise Figure	7.4 dB
	IIP3	-14 dBm
Filter	Gain	16.77 dB
	Bandwidth	1 Mhz
	Blocking @ 3 ± 1 Mhz	-20 dB
Demodulator	SNR for BER= 0.1%	29 dB
ΣΔ D/A	Resolution	8 Bits
PLL	Settling time	65μs
	VCO Phase noise	–111dBc/Hz @ 1Mhz

11.1 Recommendations for Future Work

The proposed transceiver uses the open loop modulation by directly sending modulation signal to VCO. As with fractional-N PLL a resolution of about 10 hz could be achieved, a more stable way of doing this open loop modulation would to be send the modulation signal to the dividers. But the loop bandwidth limits the frequency deviation and distorts the modulated output. To remove those distortions, a wider bandwidth PLL or some kind of compensation circuit will be required.

Also in present design inductors were used in various blocks to generate matching. These inductors consume a lot of area and have a very low Q value. So circuit topologies needs to be found, which would work without those inductors and still give equivalent performance. Inductors are also used in oscillators, they could be eliminated by designing a ring oscillator which would give a very low phase noise.

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