XGamesStation Micro Edition Cheat Sheet

Jeff Tranter <tranter@pobox.com> Version: 13-Feb-2006

General:
Program memory: 4096 12-bit words, 8 pages 512 words.
Data memory: 8-bit registers, 16 banks of 16 registers per bank plus 16 global registers,

Global Registers:

$00	INDF
$01	RTCC
$02	PC
$03	STATUS
$04	FSR
$05	RA
$06	RB
$07	RC
$08	RD
$09	RE
$0A	
$0B	
$0C	
$0D	
$0E	
$0F	

STATUS Register:

PA2	PA1	PA0	TO	PD	Z	DC	C

PA2-PA0 – program memory page select
TO – watchdog timeout
PD – power down
Z – zero
D – digit carry
C – carry

MODE Register Values (common modes only):

MODE	Access	!RA !RB !RC !RD !RE
$0C	Read	ST (0=Schmitt, 1=CMOS/TTL) [Not RA]
$0D	Read	LVL (0=CMOS, 1=TTL
$0E	Read	PLP (0=pullup, 1=no pullup)
$0F	Read	Direction (0=output, 1=input)
$1C	Write	ST (0=Schmitt, 1=CMOS/TTL) [Not RA]
$1D	Write	LVL (0=CMOS, 1=TTL
$1E	Write	PLP (0=pullup, 1=no pullup)
$1F	Write	Direction (0=output, 1=input)

OPTION Register:

RTW	RTE_IE	RTS	RTE_ES	PSA	PS2	PS1	PS0

RTW - 0=$01 is W, 1=$01 is RTCC
RTE_IE - RTCC rollover int. enable (0=enabled)
RTS - RTCC trigger selection (0=internal,1=ext. pin)
RTE_ES - RTCC input edge select (0=low to high)
PSA - prescaler assignment (0=RTCC,1=WD)
PS2-PS0 - Prescaler divide-by factors

Instruction Set:

ADD	AND	BANK	CALL	CLR	CLRB	CLZ
DEC	DECSZ	INC	INCZ	IREAD	JMP	MODE
MOV	MOVSZ	NOP	NOT	OR	PAGE	RET
RETI	RETIW	RETP	RETW	RL	RR	SB
SCSETB	SKIP	SLEEP	SNB	SUB	SWAP	TEST
XOR						

XGS Port Usage:

RA0	JOY_CLK	Joystick shift register clock (output)
RA1	JOY_SH/LD	1=shift mode 0=load mode (output)
RA2	JOY_DATAOUT	Joystick serial data out (input)
RA3	SND_SCLK	BU8763 Sound chip serial clock (output)
RA4	SND_SDATA	BU8763 Sound chip serial data (output)
RA5	SND_SSTB	BU8763 Sound chip serial strobe (output)
RA6	SND_FREQ_SEL	BU8763 Sound chip frequency select (output)
RA7	IPC_SX52_TXD	Interprocessor Communication to SX20 RB1 (bidirectional)

RB0		Unused
RB1		Unused
RB2		Unused
RB3	SX52_KBMS_CLOCK	PS/2 keyboard/mouse clock (bidirectional)
RB4	SX52_KBMS_DATA	S/2 keyboard/mouse serial data (bidirectional)
RB5	SERIAL_RXD	To serial i/o expansion port
RB6	SERIAL_TXD	To serial i/o expansion port
RB7	SRAM_BANKSEL	Static RAM bank 0=lower 64K bank, 1=upper bank (output)
RB7	IPC_SX52_RD	Interprocessor Communication to SX20 RB2 (bidirectional)

RC0	SRAM_A0	Static RAM address bus line A0 (output)
RC1	SRAM_A1	Static RAM address bus line A1 (output)
RC2	SRAM_A2	Static RAM address bus line A2 (output)
RC3	SRAM_A3	Static RAM address bus line A3 (output)
RC4	SRAM_CLK	Static RAM serial clock for address shifter (output)
RC5	SRAM_DATAIN	Static RAM serial input for address data (output)
RC6	RAM_/CE	Static RAM chip enable 0=enabled, 1=disabled (output)
RC7	SRAM_RD/WR	Static RAM read/write (0=write, 1=read) (output)

RD0	SRAM_D0	Static RAM data bus line D0 (bidirectional)
RD1	SRAM_D1	Static RAM data bus line D1 (bidirectional)
RD2	SRAM_D2	Static RAM data bus line D2 (bidirectional)
RD3	SRAM_D3	Static RAM data bus line D3 (bidirectional)
RD4	SRAM_D4	Static RAM data bus line D4 (bidirectional)
RD5	SRAM_D5	Static RAM data bus line D5 (bidirectional)
RD6	SRAM_D6	Static RAM data bus line D6 (bidirectional)
RD7	SRAM_D7	Static RAM data bus line D7 (bidirectional)

RE0	VID_ISEL0	Video Luminance (brightness) bit 0 (output)
RE1	VID_ISEL1	Video Luminance (brightness) bit 1 (output)
RE2	VID_ISEL2	Video Luminance (brightness) bit 2 (output)
RE3	VID_ISEL3	Video Luminance (brightness) bit 3 (output)
RE4	VID_CSEL0	Video Chrominance (color) bit 0 (output)
RE5	VID_CSEL1	Video Chrominance (color) bit 1 (output)
RE6	VID_CSEL2	Video Chrominance (color) bit 2 (output)
RE7	VID_CSEL3	Video Chrominance (color) bit 3 (output)

Video Brightness Levels:

Value	Brightness
0	Sync
5	Black
6	Dark Gray
10	Medium Gray
13	Light Gray
15	White

Video Color Levels (NTSC, using color 0 as color burst):

Value	Color
1	Yellow
5	Red
9	Magenta
13	Blue
15	No color burst

Typical Assembler Device Directives for XGS:

```
DEVICE   SX52
IRC_CAL  IRC_FAST
ID       'idstring'
RESET    start address
FREQ     80_000_000
DEVICE   OSCHS3
DEVICE   IFBD
DEVICE   XTLBUFD
```