

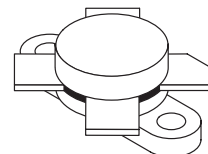
The RF Line NPN Silicon RF Power Transistor

Designed primarily for application as a high-power linear amplifier from 2.0 to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
Output Power = 100 W (PEP)
Minimum Gain = 10 dB
Efficiency = 40%
- Intermodulation Distortion @ 100 W (PEP) —
IMD = -30 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR

MRF421

100 W (PEP), 30 MHz
RF POWER
TRANSISTORS
NPN SILICON



CASE 211-11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Withstand Current — 10 s	—	30	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	290 1.66	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = 50\text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 200\text{ mAdc}$, $V_{BE} = 0$)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 200\text{ mAdc}$, $I_E = 0$)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ mAdc}$, $I_C = 0$)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 16\text{ Vdc}$, $V_{BE} = 0$, $T_C = 25^\circ\text{C}$)	I_{CES}	—	—	10	mAdc

(continued)



ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I _C = 5.0 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	10	70	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V _{CB} = 12.5 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	—	550	800	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V _{CC} = 12.5 Vdc, P _{out} = 100 W, I _{C(max)} = 10 Adc, I _{CQ} = 150 mAdc, f = 30, 30.001 MHz)	G _{PE}	10	12	—	dB
Collector Efficiency (V _{CC} = 12.5 Vdc, P _{out} = 100 W, I _{C(max)} = 10 Adc, I _{CQ} = 150 mA, f = 30, 30.001 MHz)	η	40	—	—	%
Intermodulation Distortion (1) (V _{CE} = 12.5 Vdc, P _{out} = 100 W, I _C = 10 Adc, I _{CQ} = 150 mA, f = 30, 30.001 MHz)	IMD	—	–33	–30	dB

NOTE:
1. To proposed EIA method of measurement. Reference peak envelope power.

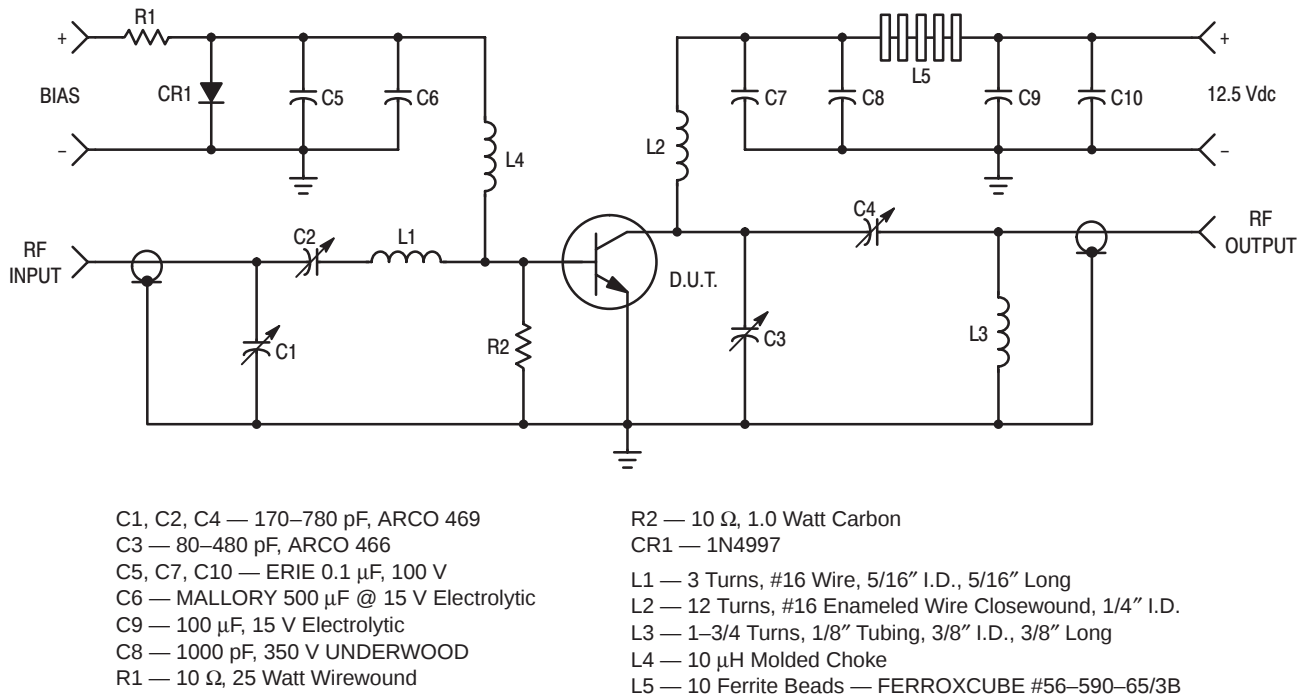


Figure 1. 30 MHz Test Circuit Schematic

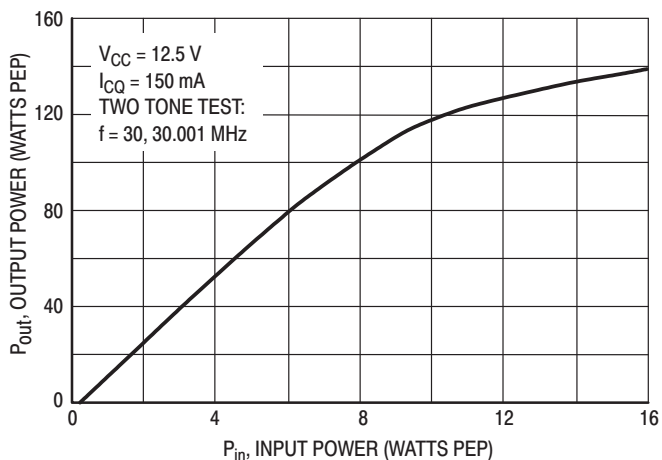


Figure 2. Output Power versus Input Power

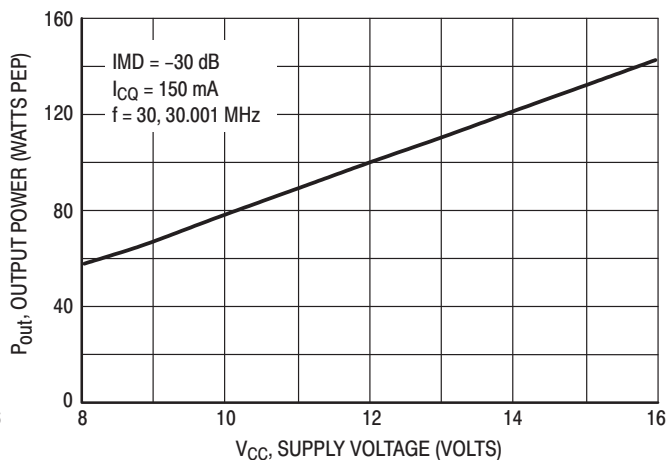


Figure 3. Output Power versus Supply Voltage

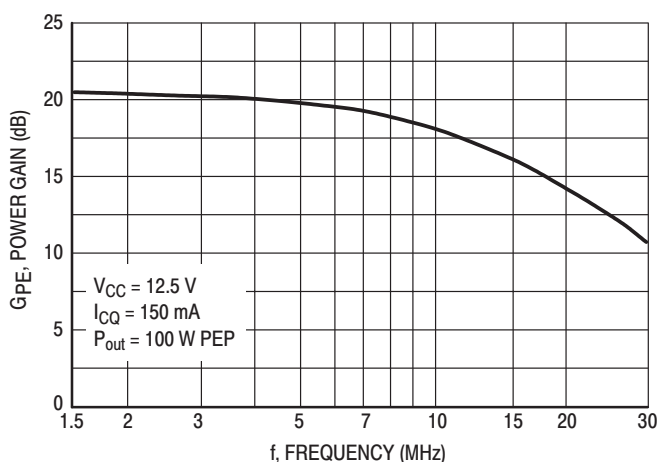


Figure 4. Power Gain versus Frequency

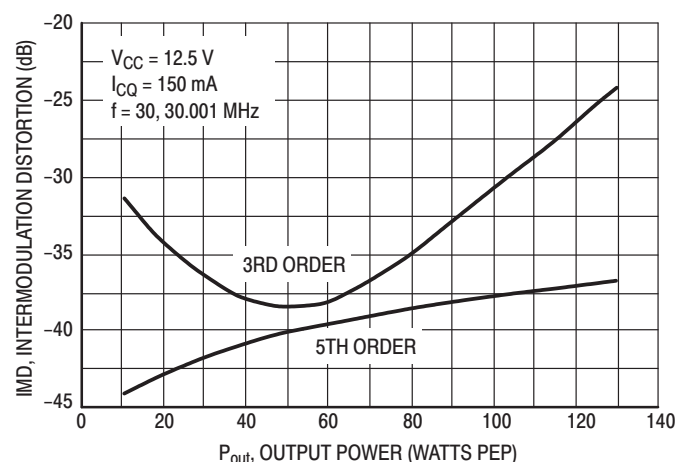


Figure 5. Intermodulation Distortion versus Output Power

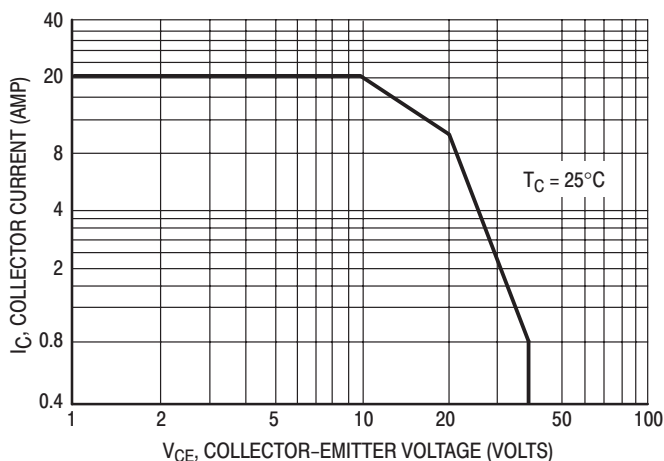


Figure 6. DC Safe Operating Area

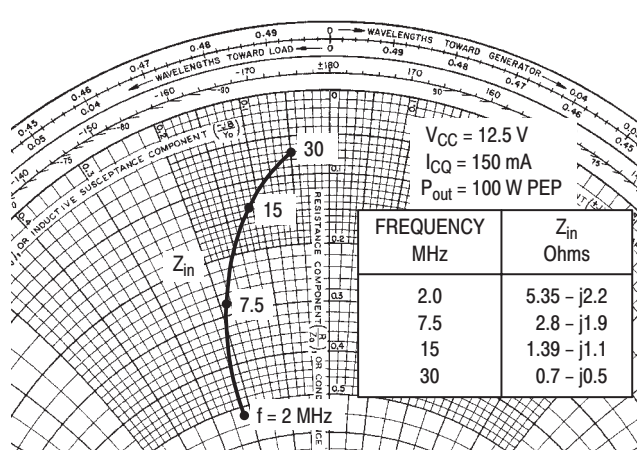


Figure 7. Series Equivalent Impedance

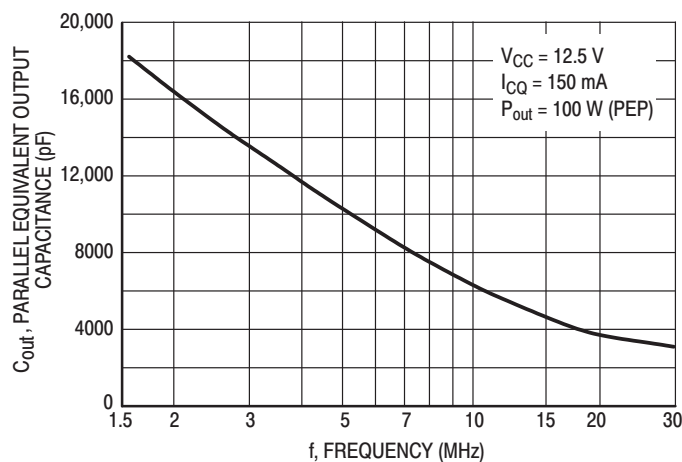


Figure 8. Output Capacitance versus Frequency

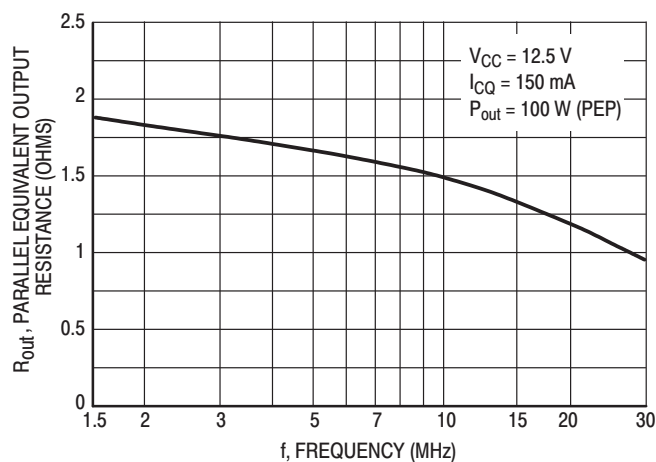
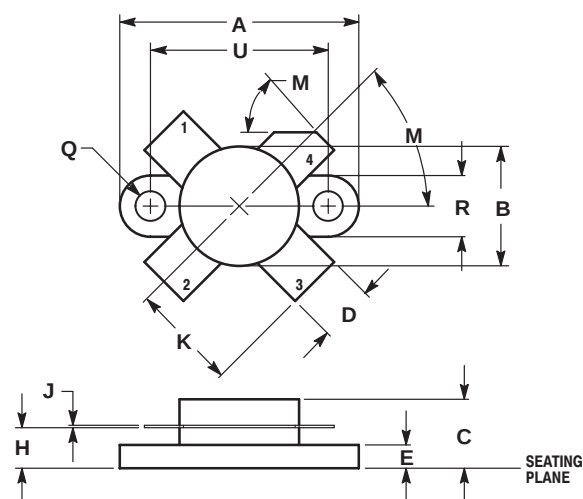


Figure 9. Output Resistance versus Frequency

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	---	11.05	---
M	45° NOM		45° NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

- STYLE 1:
1. PIN 1. EMITTER
 2. BASE
 3. EMITTER
 4. COLLECTOR

CASE 211-11
ISSUE N

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How to reach us:

USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
INTERNET: http://Design-NET.com

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



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MRF421/D

