A CMOS Implementation of the R-Transform for Translation Invariant Feature Extraction

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Abstract- **A CMOS implementation of a one-dimensional R-transform with 32 inputs is presented. The implementation generates a translation invariant feature vector from a set of spatially distributed analog inputs. Repeated application to the rows and columns of an image achieves two-dimensional translation invariance. Results are presented that demonstrate the translation invariance.**

I. INTRODUCTION

The R-transform [1], [2] is a method for generating translation invariant features from a pattern that can appear anywhere in an image. Such a transform is useful in pattern recognition applications where the position of the pattern to be classified cannot be guaranteed exactly, such as a dollar bill being inserted into a money changer, or a face being presented to a camera for identification or verification. Because a slight shift in position can adversely affect blind, rigid comparison of sensed patterns with stored exemplars on a pixel by pixel basis, the R-transform offers exceptional benefits in the tolerance of position error.

In addition to the overwhelming advantage of translation invariance in feature extraction and classification systems, the actual implementation of the R-transform is extremely well-suited for very large-scale integration (VLSI). Specifically, the implementation has two main advantages. First, only two unique functions are required, each with only two inputs. Secondly, as pointed out in [3], the functions themselves are arbitrary; the only constraint being that they are symmetrical with respect to the inputs. As a result, only a few transistors, connected in very simple arrangements similar to the differential pair, are required to implement these functions.

II. BACKGROUND

The R-transform is a member of a broader class of shift invariant transforms known as C-transforms. The R-transform is made up of many instantiations of two input-symmetrical functions connected in a fashion similar to that of the Fast-Fourier Transform (FFT), as shown in Fig. 1 and Fig. 2. The number of columns always equals the $\log_2(n)$ where n is the number of inputs equal to a power of 2. Combined with the symmetrical property of the functions, this connectivity is responsible for achieving shift invariance.

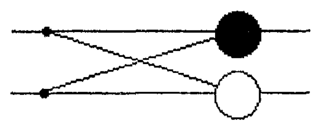

Fig. 1. A one-dimensional, 2 input R-transform, similar to the FFT butterfly. The two circles represent two unique functions, each symmetrical with respect to its inputs.

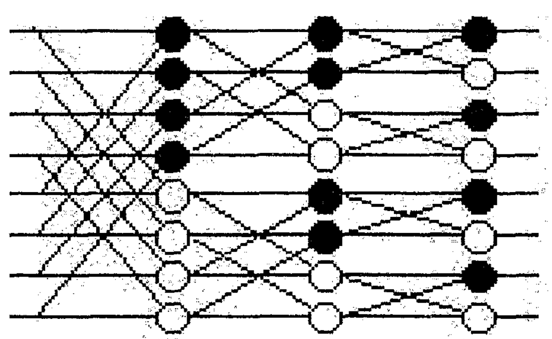

Fig. 2. A one-dimensional, 8 input R-transform for illustrating the similarity of the connectivity to that of the FFT.

The R-transform is inherently one-dimensional, but it can be extended to two dimensions as shown for the 4 x 4 case in Fig. 3. The columns are transformed first, creating an intermediate feature image, the rows of which are then transformed to produce the final feature image. The results shown in Fig. 3 were produced by two arbitrary input-symmetrical functions: 1) sum and 2) absolute value of difference.

III. METHOD

A. Transistor-Level Implementation of Input-Symmetrical Functions

Two arbitrary functions were implemented at the transistor level, as shown in Fig. 4. The circuit in Fig. 4a consists of two PFETs, m_{pa} and m_{pb}, that conduct current

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into a common transresistance node realized by the gate-drain connected NFET, m_{pc}. The output voltage, v_{o1}, develops at this node, as current is resisted. Transistors m_{pa} and m_{pb} are made to have the same width and length; therefore, the function is invariant with respect to reversing the inputs. The circuit in Fig. 4b is the same as in Fig. 4a, except the transistors are complementary to those in Fig. 4a.

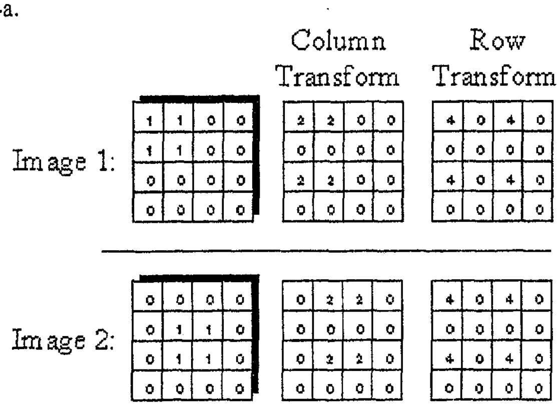

Fig. 3. Two-dimensional extension of the R-transform to the 4 x 4 case. Two images, each containing the same (shifted) pattern, generates the same feature image by applying the R-transform in two stages.

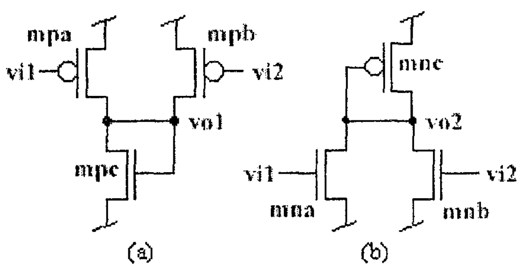

Fig. 4. Transistor-level implementation of two input-symmetrical functions. (a) P-conducting/N-resisting cell and (b) N-conducting, P-resisting cell.

The large-signal transfer functions of these two cells are shown in Fig. 5. Notice that they are somewhat complementary, which is not necessarily a requirement, but helps to generate features that are unique to the specific pattern being transformed.

B. Layout Considerations

The two circuits of Fig. 4 were laid out and connected in a 32-input arrangement as shown by the schematic of Fig. 6. The circuit consisted of five columns of 32 cells each; half of one type and half of the other.

The schematic of Fig. 6 represents connectivity only; not the actual placement of cells in silicon. Due to the fact that matching is critical in this application, care was taken

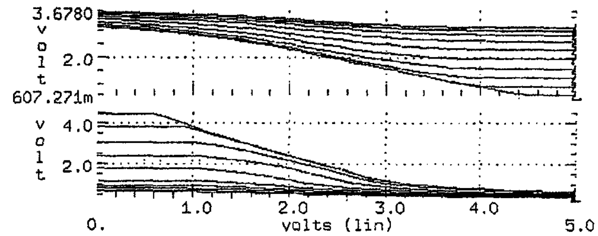

Fig. 5. Transfer functions of the two input-symmetrical functions.

to minimize variation. All cells in one layer having connections to the same cell in the 1st layer to the immediate right were placed together. After this objective was met, the set of cells having connections to the same node in the 2nd *layer to the right* as the first set of cells were placed next to the first set.

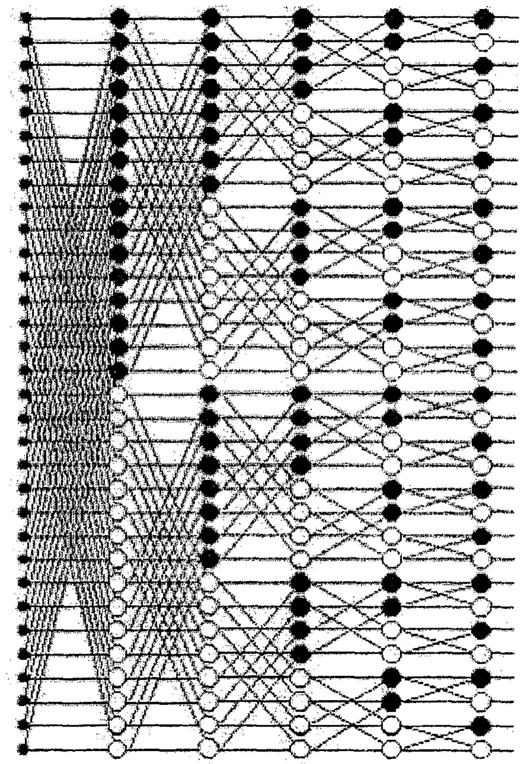

Fig. 6. Schematic of the 32-input R-transform implemented in a 2 micron CMOS process.

IV. Simulation Results

In order to demonstrate the translation invariance, a simulation was conducted that shifted a triangular pattern across the 32 inputs of the chip, one shift per microsecond. The results are shown in Fig. 7. Inputs 1, 5, 9, and 13 are shown in Fig. 7a and the first 10 outputs are shown in Fig.

7b. Although the actual inputs are different at each time step, the overall form of the pattern does not change and, as a result, the outputs do not change either; they are invariant with respect to translation.

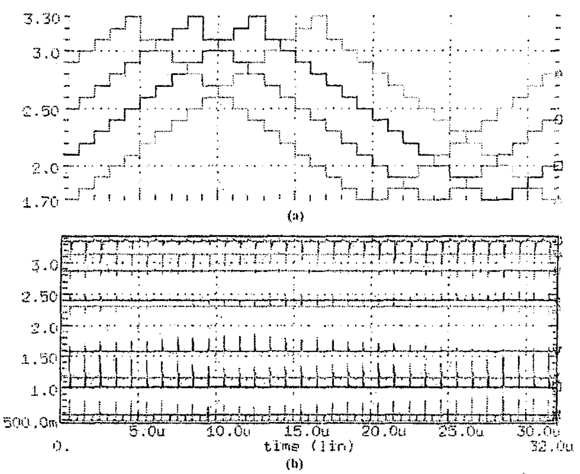

Fig. 7. Transient results of a spatial pattern being circular shifted across the 32 inputs of the R-transform. (a) inputs 1, 5, 9, and 13 showing spatial shift and (b) the first 10 outputs showing invariance.

V. Experimental Results

The chip was sent for fabrication in the standard 2 μm, double-metal, double-poly n-well ORBIT process and targeted for a 40 pin dual in-line package. A microphotograph is shown in Fig. 8. The total area was approximately 2mm x 2mm.

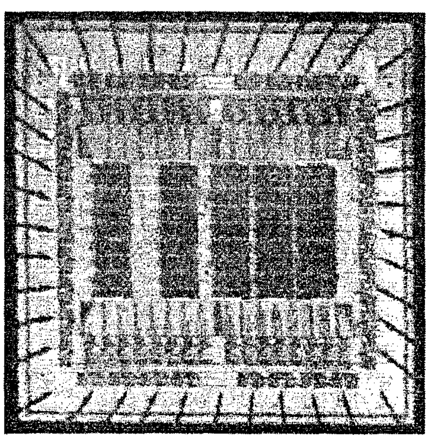

Fig. 8. Microphotograph of the 32-input R-Transform IC.

Due to a lack of pins, the inputs and outputs had to be multiplexed with switched-capacitors and the function of the 32 i/o pins was controlled by two additional pins: READ and WRITE. When WRITE was asserted, the 32 i/o pins were connected to 32 internal short-term memory (STM) capacitors. When READ was asserted, the same 32 i/o pins were connected to the 32 internal outputs for observing the resulting feature vector. In order to test for translation invariance, a programmable logic device (PLD) was programmed to alternate between two of three test patterns and their corresponding output vectors shown in Fig. 9 and Fig. 10, respectively. For a given comparison between two test patterns, the test sequence of one test set proceeded in four phases: 1) write 1st test vector, 2) read output vector, 3) write 2nd test vector, and 4) read output vector. In the 1st test set, the two patterns were made to be very different and the resulting mean squared error (MSE) between the two feature vectors was .8. In the 2nd test set, the two patterns were made to differ only by translation and the resulting MSE between the two resulting feature vectors was .016; 50 times less than the 1st case, thus demonstrating a high degree of translation invariance.

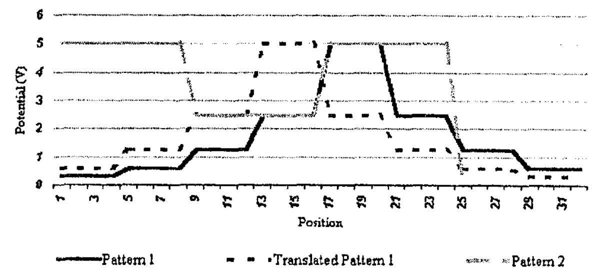

Fig. 9. Three test input patterns presented to the R-Transform IC.

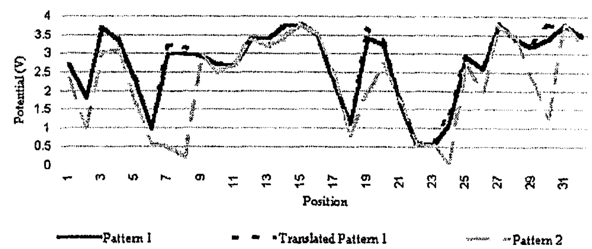

Fig. 10. Three feature vectors (output patterns) of the R-Transform IC.

References

[1] H. J. Reitboeck and T.P. Brody, "A transformation with invariance under cyclic permutation for applications in pattern recognition", *Inf. Control*, vol. 15, pp. 130-154, 1969.

[2] H. J. Reitboeck and J. A. Altmann, "Model for size- and rotation-invariant pattern processing in the visual system", *Biological Cybernetics*, vol. 51, pp. 113-121, 1984.

[3] M. D. Wagh and S. V. Kanetkar, "A class of translation invariant transforms" *IEEE Trans. ASSP* 25, pg. 203-205, 1977.