Sahil Mohan Bansal

B.E. (Senior Year), Department of Electronics & Electrical Communication,
Punjab Engineering College, Chandigarh, INDIA

PERSONAL PARTICULARS

Male, Born on 3 April, 1984 Nationality: INDIAN
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EDUCATIONAL BACKGROUND:

Pursuing Bachelor of Engineering (Electronics & Electrical Communication):

Percentage until last result declared: 70.27%
(First Division with Honors)
College: Punjab Engineering College, Chandigarh, INDIA

Intermediate (Class - 10 + 2): April 2000 - May 2002
Marks Obtained: 442/500 **Percentage:** 88.4%
(First Division with Honors)
College: DAV College, Sector 10, Chandigarh, INDIA.

Matriculation (Class - 10): April 1999 – March'00
Marks Obtained: 564/600 **Percentage:** 94.0%
Rank: Stood first among all students of the city.
School: St. Kabir Public School, Sector 26, Chandigarh.

FIELD OF INTEREST – Low Power devices and circuit design.

PROJECTS/TRAINING:

1. Eight weeks summer internship at "Institut Superieur d'Electronique des Paris", in Paris, FRANCE on "**Low power VHDL code of a 0.13 micron 500mV supply voltage based 16-bit RISC Microprocessor**" for Iris identification based security system. No. of team members: 1
2. Senior Year Major project on the design and synthesis of a "**0.13 micron 500mV supply voltage based 32-bit RISC Microprocessor incorporating clock gating**". No. of team members: 1
3. Worked on "**Minimization of variation in Id – Vds Characteristics due to Self heating of a Fully Depleted Silicon-On-Insulator MOSFET**" at Dhirubhai Ambani Institute of Information & Communication Technology (DA-IICT), Gandhinagar. No. of team members: 1
4. Eight weeks summer training at Semiconductors Complex Limited, Mohali during May-July 2004 on the **Design of 0.8u Cell Libraries** (102 cells) for SCL in Cadence and Tanner tools. No. of team members: 2
5. Made a wireless controlled robot that included a Line follower stage for the International Robotics Competition – Survivor – at the IIT B Techfest 2005.

No. of team members: 4.

TUTORIALS ATTENDED

1. Attended full day tutorial on **"Technology Impacts on sub 90nm CMOS Circuit design and design methodologies"** by Joshi R. and Puri R., IBM T.J. Watson Research Center, Karnik T., Intel at the 19th IEEE VLSI Design conference (2006) in Hyderabad, INDIA.
2. Attended tutorial on **"Design of Embedded Systems with Novel Applications"** by Lacovara R.C., Applied Defence Systems, USA and Vaman D.R., Prairie Viem A&M University at the 19th IEEE VLSI Design conference (2006) in Hyderabad, INDIA.
3. Attended tutorial on **"Embedded Systems design using FPGA"** by Patel P. Xilinx, USA at the 19th IEEE VLSI Design conference (2006) at Hyderabad, INDIA.
4. Attended tutorial on **"CMOS analog circuit design"** by Sharma D., IIT B, at the National Workshop on Challenges in VLSI (NWCV) 2005 at DA-IICT, Gandhinagar, INDIA.
5. Attended a full day tutorial on **"System-on-chip Design Methodology: a practical approach"** at the 18th IEEE VLSI Design conference (2005) at Kolkata, INDIA.
6. Attended a full day tutorial on **"Compact MOSFET models for low power analog CMOS Design"** at the 18th IEEE VLSI Design conference (2005) at Kolkata, INDIA.

CURRENT PROJECTS

1. Layout generation of a low power 32-bit RISC processor incorporating clock gating and other techniques for reducing power consumption.
   No. of team members: 3
2. Study of the impact of process variations on the leakage power consumption of 65nm and 45nm MOSFETs using the Berkeley Predictive Model.
   No. of team members: 1

PUBLICATIONS & PRESENTATIONS

1. Paper titled **"130nm Partially Depleted SOI for Ultra Low Power applications"** selected for presentation and publication at the 2006 IEEE Canadian Conference on Electrical and Computer Engineering, to be held in May 2006 at Ottawa, Canada. The paper presents the results of a 16-bit RISC processor using 500mV 0.13 micron FD SOI technology and shows the results of lower power consumption of the processor as compared with contemporary processors. The results were achieved using clock gating and operand isolation as power reduction techniques. I am working on expanding this work to a 32-bit RISC processor.
2. Paper titled **"FD SOI based ultra low power 32-bit RISC processor"** selected for publication in the proceedings of the 2006 IEEE Eclectica – paper presentation contest cum researchers' forum being organized at Punjab Engineering College, Chandigarh, INDIA on 10th of Feb. 2006. The paper presents design and synthesis results of a clock-gated FD SOI technology based

ultra low power 32-bit RISC processor.

3. Paper titled "**Minimizing variation in output characteristics of a FD SOI MOS due to self heating**" selected for poster presentation and publication at the "VLSI Design & Test Symposium 2005" being held from August 11-13 2005 at Bangalore, INDIA. The paper presented a feedback circuit model for reduction in the effect of temperature gradient on drain current of FD SOI MOSFET as well as proposed a novel idea of a device level implementation to achieve better results without the use of any additional circuitry. Results verified by simulation.
4. Paper tilted **"A Quantitative drain current thermal of a Fully Depleted SOI MOS"** selected for the poster session at the 16th IEEE International Conference on Microelectronics (ICM), December 6-8, 2004, Tunis, Tunisia. The project proposed a mathematical technique to accurately determine the effect of non-linear thermal gradients on the performance of SOI MOSFETs.
5. Paper titled **"Metal T-Gate Structure for Fully Depleted SOI RF-CMOS Technology"** selected for presentation & publication in the proceedings of the Indian Microelectronics Society (IMS) Conference November 19-20th 2004, organized by Punjab University, CSIO & Semi-Conductors Complex Ltd. at Chandigarh, INDIA. The paper studied the usefulness of a T-Gate SOI MOS structure and compared its performance with bulk silicon.
6. Poster presentation and abstract publication at the 1st International Conference on Advanced Nanotechnology titled **"Molecular Digital Logic Circuits"** October 23-26, 2004 organized by Foresight Institute in Washington D.C., U.S.A. The paper studied the effectiveness of making structures using benzene derivatives for implementation of basic logic gates and adders.

FELLOWSHIPS AWARDED:

1. Awarded a fellowship to attend the 18th IEEE VLSI Design Conference 2005 at Kolkata, INDIA from January 3-7, 2005.
2. Awarded a fellowship for the 19th IEEE VLSI Design Conference 2006 to be held at Hyderabad, INDIA from January 3-7 2006.

PROFESSIONAL MEMBERSHIPS AND ACTIVITIES

I E E E

1 Chairperson of Student Branch since March 2005

2. Treasurer & Membership Development Chairperson of IEEE Student Chapter Punjab Engineering College for the year 2004.

I E T E

1. Technical Committee head from 3rd year & Core Member of the IETE Students' Forum, Punjab Engineering College, Chandigarh during 2003-04.

AWARDS/ACHIEVEMENTS AND OTHER ACTIVITIES

1. Awarded the IEEE J.K. Pal Memorial award for my contribution towards the activities of IEEE Student Branch of Punjab Engineering College, Chandigarh, INDIA.
2. Achieved a score of 1490 in the GRE general test taken in March 2005. The

details of the score is Verbal – 690/800 Quantitative 800/800 Analytical Writing 5.5/6.0

3. Was a reviewer with the paper review committee of the 9th IEEE VLSI Design and Test Symposium 2005 held at Bangalore, INDIA.
4. Organized Inter-College paper presentation contest cum researcher's forum as a part of the college techfest "Eclectica 2005" from 14-15 April 2005 and "Eclectica 2006" from 10th -11th February 2006.
5. Organized Information Sharing Meetings (ISMs) on various topics such as device modeling, carbon nanotubes, low power design etc. and also organized a hardware design competition and a workshop on MATLAB as the chairperson of the IEEE Student Branch of my college.
6. Was awarded a "Credit" in "International Competition for Schools (Science)" in 1998 organized by University of New South Wales, Australia.
7. Stood 30th in a National Level Mathematics Olympiad organized by the Indian Talent Search Institute in the year1999.
8. Was placed amongst the National Top 1% students in "National Standard Examination In Physics" organized by the "Indian Association of Physics Teachers"
9. Have been an active "Youth Volunteer for Positive Living" as a part of the Commonwealth Youth Program fighting against AIDS & Drug Abuse.
10. Have been actively involved in the "Commonwealth Youth Credit Initiative" (CYCI) scheme as a part of the NSS program in the college.
11. Have been a part of the college placement office for the last three years as the representative of Electronics and Electrical Communication Department.
12. Was awarded the Appreciation award for commendable work as the member of college English Editorial Board.

HOBBIES

I like to read books and novels, listening to soft music, watching cricket, soccer and F1 racing. I like to play table tennis and am also learning to play the guitar.

(SAHIL M BANSAL)