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Amorphous Silicon Direct Bonding (a-SDB) with Improved Surface Roughness

Bong-Hwan KIM*, Taek-Dong CHUNG‡, Jong-Won LEE‡, Yong-Jae LEE and Kukjin CHUN

Inter-university Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National University, Seoul 151-742
†*Institute of Medical and Biological Engineering, Medical Research Center, Seoul National University, Seoul 110-799*
‡*Micro System Team, Electronic Materials Laboratory, Institute for Advanced Engineering, Yongin 449-820*

In this paper, we realize direct bonding between amorphous silicon and various silicon dioxide layers. The 1 μm thick amorphous silicon layer deposited by LPCVD at 550 °C and 6000 Å thermal SiO_2 on silicon substrate form direct bonds. The 1600 Å CVD SiO_2 layer deposited by PECVD can also make direct bonding with amorphous silicon. This is an advanced silicon direct bonding technology and is suitable for the design of silicon micro-machined structures.

I. INTRODUCTION

Silicon direct bonding (SDB) is a bonding technique of two silicon wafers together with homogeneous or heterogeneous layers without the use of any intermediate adhesives. The SDB technique simplifies the process and cost by reducing mask level, and its necessity has increased in terms of its fields of applications such as power devices, SOI, sensors and actuators. Factors which can affect direct bonding between silicon wafers are wafer curvature, flatness, contamination and roughness of the surface among which roughness is very important. For effective wafer bonding, surface roughness must be less than 5 Å [1–3]. When the polysilicon layer used for most of MEMS structures on wafer has high roughness, conventional treatment yields so weak a bond that direct bonding between two wafers with polysilicon layer is rarely formed. The same phenomena has been reported for CVD oxide [1]. For reason that amorphous silicon is able to make polysilicon by annealing process, we propose amorphous silicon direct bonding (a-SDB) using a reduced roughness of surface. Amorphous silicon has less than 5 Å surface roughness and the a-SDB is completely compatible with subsequent high temperature process operations such as oxidation and diffusion because of the well matched thermal expansion coefficients of the bonded layers and very low thermal stress. This technique will be adapted for integrated microlens with multi-electrode focusing lens, amorphous silicon TFT and isolation of power device. In this paper, we will also investigate roughness criterion of bonding interface for amorphous and polysilicon as well as CVD oxide.

II. FABRICATION

The mechanism of SDB between two wafers was proposed by R. Stengl, *et al.* [4,5]. From room temperature to 200 °C, the initial bonding in room temperature takes place as a result of interaction between Si-OH group which is formed by wafer cleaning. Bonding force increases by heating up to 700 °C and Si-OH bonds are changed to Si-O-Si bonds by dehydration in Si-OH groups. Oxygen at the interface diffuses inside the silicon bulk, and Si-Si bonds are formed above 1000 °C. The a-SDB is considered to follow the bonding mechanism of the SDB. The a-SDB was carried out in the following process. First, 1 μm thick amorphous silicon was deposited on silicon wafer with LPCVD at 550 °C on 6000 Å thermally grown silicon dioxide to yield a 1 μm layer and while the other wafer had the same 6000 Å thickness silicon dioxide on the surface. The wafers were immersed into an oxidizing solution at 120 °C for 10 minutes, which was composed of H_2SO_4:H_2O_2=4:1 in volume. Then, the wafers were RCA cleaned and rinsed in deionized water for 10 minutes. Hydrophilic silicon wafers were dipped into 10:1 HF after RCA cleaning. Then immersing again into the same solution for 10 minutes brought about a change in the surface. Two wafers were carefully attached to each other at room temperature for 5 minutes. Finally, annealing in a furnace for 2 hours completed the a-SDB process.

III. RESULTS & DISCUSSION

1. Bonding Layers

*E-mail: bhkim@ssel.snu.ac.kr, Tel: 82-2-880-5451(ext. 256),
Fax: 82-2-887-6575

Table 1. Roughness of amorphous silicon and polysilicon

Type of wafer surface	Room temperature at initial bonding	High temperature annealing
Si/Si	bonded	bonded
Si/SiO_2	bonded	bonded
SiO_2/SiO_2	bonded	bonded
a-Si/Si	bonded	bonded
a-Si/SiO_2	bonded	bonded
a-Si/a-Si	bonded	bonded
Poly-Si/Si	bonded	not bonded
Poly-Si/SiO_2	bonded	not bonded
Poly-Si/Poly-Si	not bonded	not bonded

Table 2. Result of silicon direct bonding

Wafer surface	Peak-to-peak	rms roughness	Average roughness
a-Si 1μm @550 °C, wet SiO_2 0.5μm Si	60.1 Å	3.88 Å	2.74 Å
Poly-Si 1.8μm @580 °C Wet SiO_2 1.6μm Si	117 Å	9.18 Å	6.01 Å
Wet SiO_2 1000 Å Poly-Si 1.8μm @625 °C Wet SiO_2 1.6μm Si	3380 Å	451 Å	354 Å
Poly-Si 2μm @625 °C Wet SiO_2 1.6μm Si	3160 Å	505 Å	403 Å

In the experiments, we found several layers that could bond together and they are summarized in Table 1. The Si/Si, Si/SiO_2, and SiO_2/SiO_2 layers were well bonded as reported in papers [1–7]. In addition, amorphous silicon layer was well bonded to Si, SiO_2, and amorphous silicon. However, it was difficult to bond a polysilicon layer to Si, SiO_2, and polysilicon.

2. Void & Roughness

The a-SDB generates more voids compared to the SDB at high temperature because of high roughness. Fig. 1 displays the surfaces of deposited silicon layers for different temperatures. At 625 °C, the roughness of polysilicon surface is worse than that at 580 °C . As indicated in Table 2, the thinner the polysilicon layer and the lower the deposition temperature, the lower the surface roughness. Figure 2 shows the transmitted IR images of the a-SDB wafers. The voids are distributed for 20∼30 % in 4 inch wafer. However, The voids in figures (c), (d), and (e) could be removed with another annealing except (b) since there is no channel for the extraction. In Fig. 3, we notice that voids are extracted for another 2 hours of annealing in the furnace at 1000 °C. Fig. 4 displays

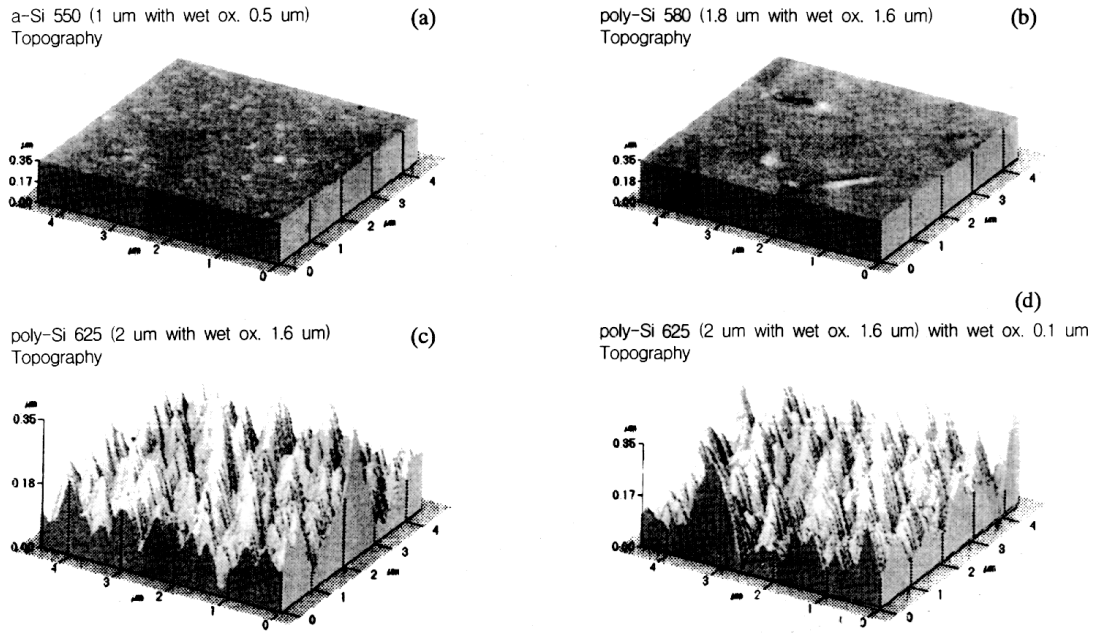

Fig. 1. Surface topography of wafer measured by AutoProbe X5. (a) a-Si 1 μm @550 with thermally grown silicon dioxide on bulk silicon. (b) Poly-Si 1.8 μm @580 °C with the same 1.61 μm silicon dioxide. (c) Poly-Si 2 μm @625 °C with the same 1.6 μm silicon dioxide. (d) 1000 Å thermally grown silicon dioxide on Poly-Si 2 μm @625 °C with the same 1.6 μm silicon dioxide.

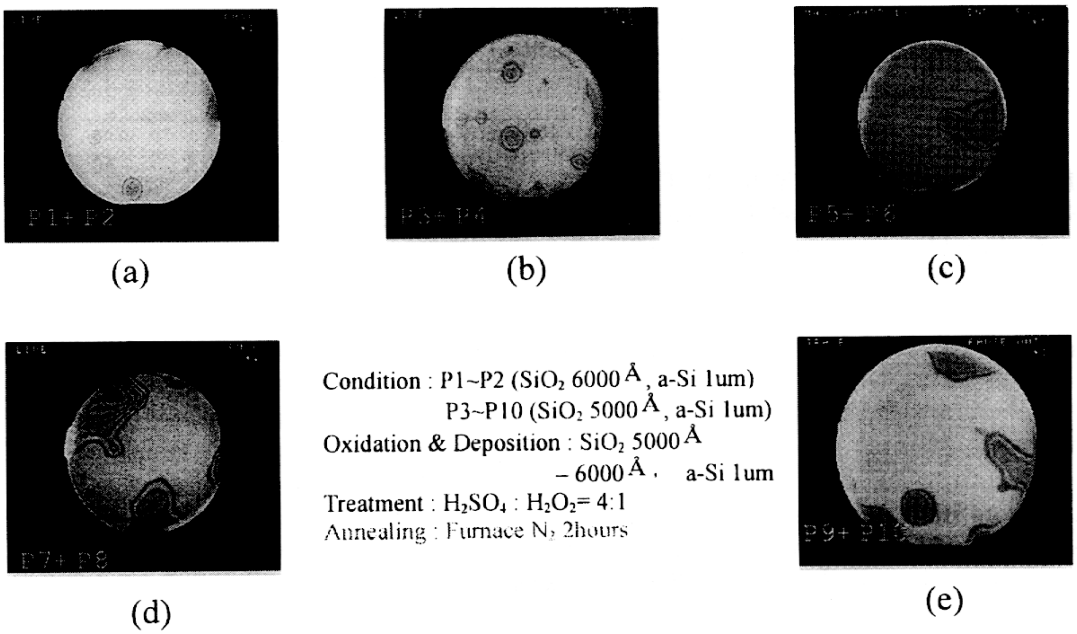

Fig. 2. Photographs of wafers from the amorphous silicon direct bonding results. (a) 1 μm a-Si & 6000 Å thermal oxide. (b), (c), (d), and (e) 1 μm a-Si & 5000 Å thermal oxide.

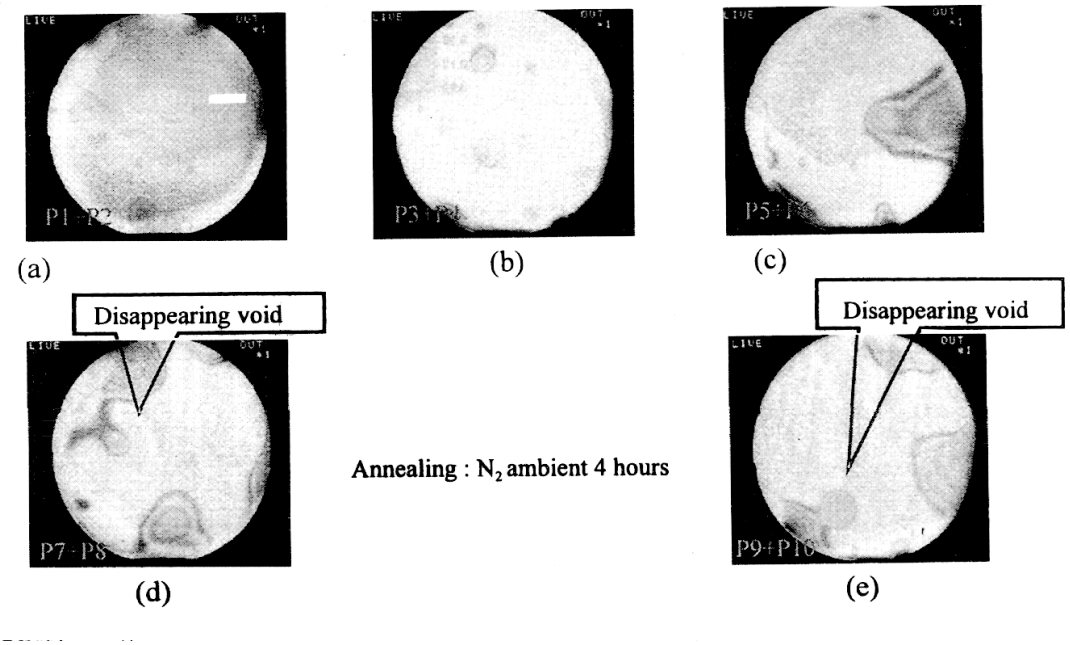

Fig. 3. Disappearing void in a-SDB from another two hours of annealing. (a) 1 μm a-Si & 6000 Å thermal oxide. (b), (c), (d), and (e) 1 μm a-Si & 5000 Å thermal oxide.

a cross-sectional view of scanning electron microscope (SEM) of two bonded wafers interface. In Fig. 4(c), Interfacial amorphous silicon and thermal oxide are visible. We can also see that interface dislocations are absent.

3. Surface Energy

The surface energy, γ, can be evaluated as in equation (1) from the wafer edge by crack propagation method using razor blade [7].

$$\gamma = \frac{3}{8}\frac{Et^3y^2}{L^4} \tag{1}$$

Where E is the elasticity, t is the thickness of the wafer

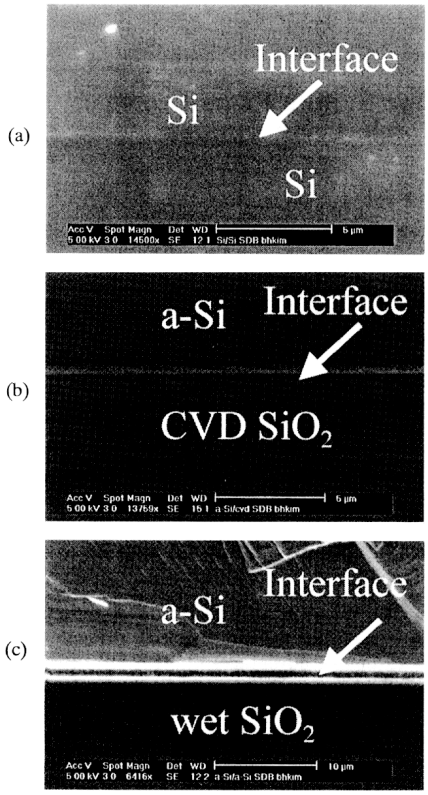

Fig. 4. Cross-sectional view of scanning electron microscope (SEM) of two bonded wafers interface. (a) direct bonding between Si and Si. (b) CVD oxide and 1000 Å a-Si on 1000 Å thermal oxide. (c) 1 μm a-Si on 6000 Å thermal oxide and 6000 Å thermal oxide.

and L is the crack length. The surface energy of bonding wafers were found to be 0.7∼0.8 [J/m^2] at 500∼700 °C and 1∼1.5 [J/m^2] at 900∼1000 °C, which were close to the previously reported results [8].

IV. CONCLUSIONS

Polysilicon direct bonding is a very difficult process due to roughness problem, which can be eliminated by chemical mechanical polish. Amorphous silicon looks promising in terms of reducing the roughness, which is the most important factor in bonding. The amorphous silicon direct bonding can be used instead of polysilicon for various MEMS structures for this reason. However, when amorphous silicon is doped with $POCl_3$, its roughness tends to increase due to continuous grain growth, which can be eliminated by *in situ* doping.

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