A 165 MS/s 8-bit CMOS A/D converter with background offset cancellation

G. Feygin, K. Nagaraj, R. Chattopadhyay, R. Herrera, I. Papantonopoulos[1], D. Martin, P. Wu and S. Pavan
Texas Instruments, Warren, New Jersey and Dallas, Texas[1]

Abstract

A 8-bit A/D converter using an efficient architecture is described. An important feature of this is a background offset cancellation scheme. This A/D converter has been implemented in a $0.18\mu m$ digital CMOS technology. It operates at up to 165 MS/s with an SNDR of 43.5 dB, a DNL of 0.7 LSB and an INL of 1 LSB. It occupies an active area of $0.9mm^2$ and has a power dissipation of 140 mW.

I. Introduction

High speed A/D converters with 8-10 bits of resolution are required for video signal processing and data communication applications. A conventional full flash architecture, while being capable of operating at high speeds, is expensive in area and power. This paper will describe an 8-bit A/D converter that uses an area and power efficient architecture built around a 6-bit flash core. It employs a background comparator offset cancellation scheme that lends itself to the use of simple, low power circuits in realizing the 6-bit core.

II. Architecure of the A/D converter

A block schematic of the A/D converter is shown in Fig. 1. A 6-bit core produces the 6 middle bits. The most significant bit (MSB) is obtained from the front end that precedes the 6-bit core. The input is simultaneously sampled by a fully differential sample and hold (S/H) circuit as well as by a polarity detector which is essentially a zero crossing detector (ZCD). The output of the ZCD controls a polarity reverser that is inserted at the output of the S/H. Whenever the input sample is negative, the polarity of the S/H output is reversed. Thus, the 6-bit core only sees positive signals, effectively doubling its resolution. The output of the ZCD gives the MSB. Taking advantage of the differential architecture, the polarity reversal is realized simply by cross-connecting the positive and negative signals from the front end into the 6-bit core.

The least significant bit (LSB) is obtained by means of a special two-step operation [1] as illustrated in Fig. 2. The S/H samples the input when the clock signal CK1 is high. The output is held for an entire clock cycle, to maximize the time available for conversion. During the first step, a 6-bit A/D conversion is performed with an analog voltage equal to 1 LSB (or 1/2 LSB of the 6-bit core) added to the output of the S/H. The 6th bit from this operation is stored in a 1-bit memory element. During the second step a 6-bit A/D conversion is performed without the offset added to the input. If the input were to lie in the upper half a code interval of the 6-bit core, adding the offset would push the result of the conversion into the next higher digital code. Thus, the results from the first and second steps would be different. This condition is detected by means of an exclusive-OR operation between the 6th bits from the two steps, to generate the LSB. Each conversion step consists of a 'reset' phase followed by a 'convert' phase. The addition of the 1 LSB voltage is achieved by means of a small resistor in series with the input to the comparator array. A reference current is forced through this resistor whenever the 1 LSB offset is required [1].

Two features distinguish this approach from traditional two-step approaches [2-3]. First, the decision from the first step is not required for the second step. Secondly there is no significant change in the analog voltage or any major circuit switching that occurs during the second step. This allows the second step to me much shorter than the first step, thus enhancing the speed of operation. The non-uniform clock phases shown in Fig. 2 are derived using a delay lock loop (DLL). The falling edge of CK1 is slaved directly to the input clock, eliminating any sampling error due to phase jitter in the DLL.

III. Front-End

A circuit schematic of the S/H circuit is shown in Fig. 3. CK1 and CK2 are non-overlapping clock phases. When CK1 is high, the input is sampled on C1P and C1N. During the time CK2 is high an amplification is performed by transferring the input charge to capacitors C2P and C2N. Simulatneously the output of the opamp is sampled by C3P and C3N. When CK1 goes high again, C3P and C3N are connected across the opamp, causing the output voltage to be held for a full clock period. The output of the S/H circuit is buffered by source follower buffers M1 and M2 which drive the comparator array. The opamp employs a telescopic cascode architecture to achieve the bandwidth required for this application.

The ZCD consists of an input sampling network followed by a latch whose output gives the polarity signal. An important issue here is the error between the input sensed by the S/H and that sensed by the ZCD. Two sources of this are the sampling instant error and offsets in the ZCD. The sampling instant error is minimized by making the sampling network in the ZCD identical to that in the S/H . The offsets are minimized by a proper choice of transistor sizes in the ZCD. Any residual error is eliminated by employing a redundancy in the comparator array, as will be described later.

IV. 6-Bit Core

The overall structure of the 6-bit core is shown in Fig. 6. Although not shown in the figure, the analog signal path is fully differential. The main comparator array performs 6-bit conversion by comparing the input to reference voltages derived from a resistive ladder. The differences are amplified by the preamps and then latched by the latches.

To reduce the input capacitance of the comparators and to save area and power, the preamps use interpolation to eliminate half of the first stage of preamps. Thus, for 6-bit conversion we would only need 32 first stage preamps, 64 second stages preamps and 64 latches. However in this implementation we use 34 first stage preamps, and 68 second stage pre-amps and latches. The extra comparators are used for providing redundancy to correct for any errors in the polarity detection, as discussed in section III. In addition to this we also have an auxiliary comparator array which is used for background offset cancellation in the main array, as will be described in section V.

Preamp Stages

The operation of the first stage preamp (P1) is shown in Fig. 4(a). During an autozero period (AZ), the reference voltages, produced by a resistor ladder, are connected to one side of the input capacitors while

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feedback loops are connected around the preamp. The voltage stored on the capacitors is equal to the reference voltage minus the input referred offset voltage of the preamp. For conversion cycles, the feedback around the preamp is opened, and the capacitors are connected to the S/H output instead of the resistor ladder.

The circuit schematic for P1 is shown in Fig. 5. It employs a fully differential folded cascode architecture. Common mode feedback is provided by connecting the output nodes to the gates of the tail current transistors M1 and M2. A folded cascode circuit rather than a simple single stage differential amplifier is used to minimize any offset due to the kick-back from the output of the pre-amplifier to its input. This is important because in this architecture where the front end consists of a polarity reverser, any offset in the 6-bit core would translate into a large differential non-linearity (DNL) at the mid-code.

The preamp is reset during the first part of every clock cycle by turning on the reset switch. As soon as the reset goes low, the amplifier simply 'integrates' the input and the output grows until the end of the clock cycle. This integrating architecture minimizes the power required to achieve a desired dynamic gain. It also has a larger DC gain that enables better offset cancellation.

The architecture of the second stage preamp is shown in Fig. 4(b). It has two main differential input pairs to facilitate interpolation, and an auxiliary differential input for offset cancellation [1]. During the autozero period the inputs are zeroed and the output is fed back to the auxiliary input, and the resulting error voltage is stored on grounded capacitors connected to the auxiliary input.

V. Background Offset Cancellation Scheme

An essential feature of the above comparator array is that the preamps use offset cancellation. This allows the use of very small devices sizes which in turn minimizes the area and power. However, one disadvantage of offset cancellation is that an autozero interval is needed for this purpose. One way of accomplishing this without interrupting conversion is to use one or more extra comparators that can substitute for the comparators that are being autozeroed. This way, we can autozero all the comparators sequentially. In the case of a full flash converter this can be done using a single extra comparator [4]. However, with interpolation, a single comparator can not be autozeroed by itself. For the comparator array shown in Fig. 6, at least 5 comparators have to be taken out of service at a time. This is because in order to autozero one of the interpolating second stage preamps, the two first stage preamps connected to the have to be reset. This in turn disables the four other second stage preamps connected to these. Thus, the auxiliary comparator array has to be able to replicate five comparators at a time. It can be seen that to do this, it will have to have four first stage preamps and five second stage preamps and latches. It is very important to accomplish the switching between the autozero mode and the normal mode with minimal disruption of the sensitive parts of the main comparator array. A scheme that achieves this has been implemented, as described below.

Operation of the comparators during autozero

Before a group of comparators is removed from the main array, the auxiliary comparators are autozeroed to reference voltage corresponding to the comparators they are going to replace. This process is illustrated in Fig. 6. Let us assume that we wish to autozero comparators k through k+4. The corresponding reference voltages from the reference ladder are connected to the auxiliary comparator array by means of a reference bus that runs along the main comparator array on to the auxiliary comparators. During this interval the digital outputs from the auxiliary array are ignored. Next, main comparators k through k+4 are autozeroed, while they are replaced by the auxiliary comparators.

Once comparators k through k+4 are autozeroed, it is the turn of comparators k+2 through k+6. This overlap between successive groups is required to make sure that all the preamps are covered.

Operation of the digital back end during autozero

In a flash A/D converter the comparator array generates a thermometer code output which is converted into a 1 of 2^n code by a logic that detects the transition from all '1's to all '0's in the thermometer code. To replicate this function in the autozero mode, we would have to physically replace the the digital outputs of main comparators k through k+4 with the the outputs of the auxiliary comparators. This would require a set of 5 signals to run from the auxiliary comparators along the entire main comparator array. The resulting large parasitic capacitance would severely limit the speed of operation of the A/D converter. Further, because of the overlap between successive groups of autozeroed comparators, each output in the main array would have to select from a main comparator or one of three comparators in the auxiliary array. This requires a 4-way multiplexing operation which again slows down the operation. These problems are avoided in the present implementation by completely bypassing the comparators k through k+4 when they are being autozeroed. This is done by 'shifting down' the outputs of all the comparators above k+4 by 5 levels, as shown in Fig. 7. Thus, the output of the main comparator array now comprises a modified thermometer code which has the following properties. If the input sample is below code k, the binary output from the main comparator array would be the same as that during normal mode, whereas the output of the auxiliary array would be zero. If the input sample falls above code k+4, the output from the main comparator array would be 5 less than that during the normal mode, whereas the output of the auxiliary array would be 5. If the input sample is between codes k and k+4, the output of the main comparator array would be k -1 whereas the output of the auxiliary array would be between 1 and 5, depending on the exact value of the input. For all of the above cases the correct output is obtained simply by adding the binary output from the main array to the binary output from the auxiliary array, as is done in Fig. 7.

With this arrangement, the only physical change that occurs in the back end of the main array during the autozero mode is the downward shifting of all the comparator outputs above the level k+4. This only requires short, local wiring that does not add a significant amount of parasitic capacitance. Also, only a 2-way multiplexing of the comparator outputs is required.

The propagation of the autozero cycle through the array is achieved by means of a central autozero controller with the help of a small amount of control circuitry in each comparator. .

VI. Reference Pre-distortion

In order to meet the gain error specification, the full scale reference voltage applied to the reference ladder must exactly equal the full scale output of the S/H circuit. Any gain error in the S/H circuit must be accounted for in generating the reference voltage. The basic S/H circuit itself is free from gain error, but the buffers that follow it have gain that is affected by body effect in the source followers as well as by the finite output impedance of their tail current sources. To compensate

for this, the reference voltages to the ladder are pre-distorted by using a replica circuit as shown in Fig. 8. Here V_{max} and V_{min} are the full scale voltages referred to the output of the S/H just before the buffers. Transistors Mb1 and Mb2 are replicas of the sources follower buffers (M1 and M2 in Fig.3). Two simple, single stage amplifiers are used around Mb1 and Mb2, constituting 'super source followers' that drive the reference ladder. The reference seen by the ladder is now exactly equal to the full scale signal range at the output of the front end. This scheme also automatically ensures that the common mode level of the reference ladder is exactly equal to the output common mode level of the front-end.

VII. Experimental Results

This A/D converter has been implemented in a 0.18 μm, 4-level metal digital CMOS technology. A microphotograph of the device is shown in Fig. 9. It occupies an active area of 0.9 mm^2. The measured performance is summarized in Table 1. The output spectrum with a sampling frequency of 165 Ms/s and an input frequency of 10 MHz, is shown in Fig. 10. The measured signal to noise + distortion ratio (SNDR) is about 43.5 dB at 10 MHz and is about 42 dB at 80 MHz. The spurious free dynamic range (SFDR) is 53 dB. The measured differential non-linearity (DNL) and integral non-linearity (INL) are shown in Fig. 11. The device uses a dual supply voltage (3.3V and 2V). The power consumption excluding the output drivers, is 140 mW. The output drivers consume an additional 65 mW.

References

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Table 1 : Summary of performance

Technology	0.18 μm 4-level metal CMOS
Active area	0.9 mm^2
Supply voltage	3.3V/2V
Sampling frequency	165 MS/s
SNDR at fin = 10 MHz	43.5 dB
SNDR at fin = 40 MHz	42 dB
SNDR at fin = 80 MHz	42 dB
SFDR	53 dB
DNL	0.7 LSB
INL	1 LSB
Power dissipation	140 mW

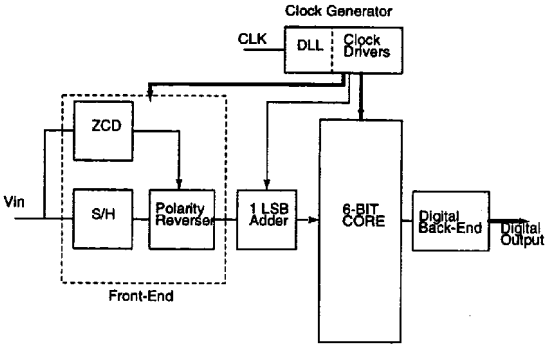

Fig. 1. Block schematic of the A/D converter

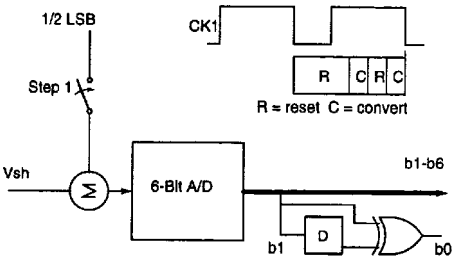

Fig. 2. Generation of the LSB

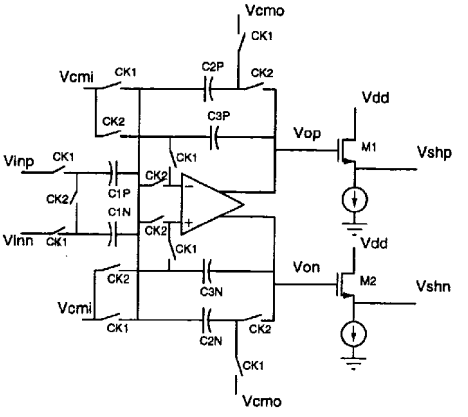

Fig. 3. Circuit schematic of the S/H circuit

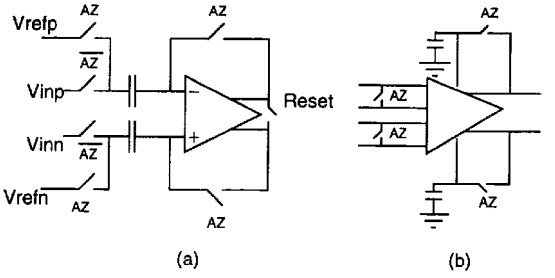

Fig. 4. Operation of the preamps (a) First stage and (b) Second stage

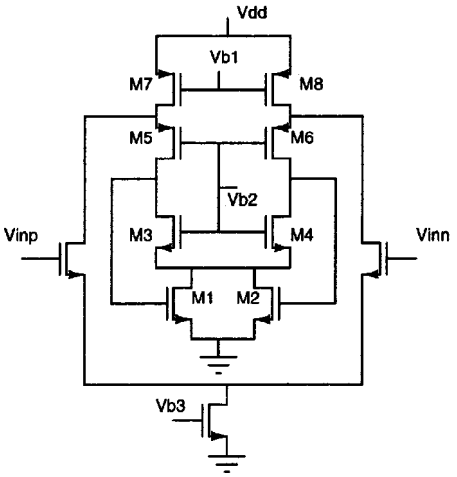

Fig. 5. Circuit schematic of the first stage preamp

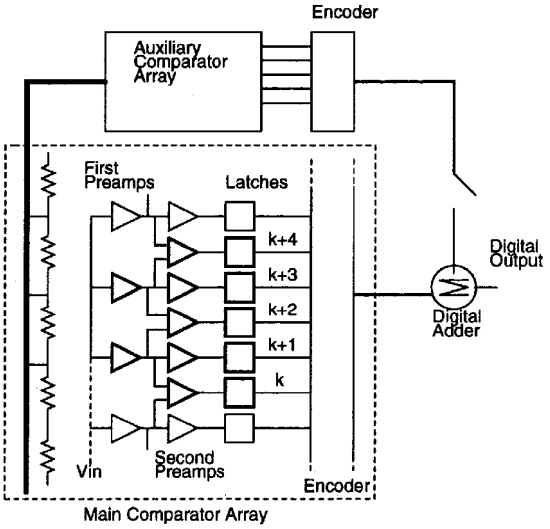

Fig. 6. Configuration during the first part of an autozero cycle

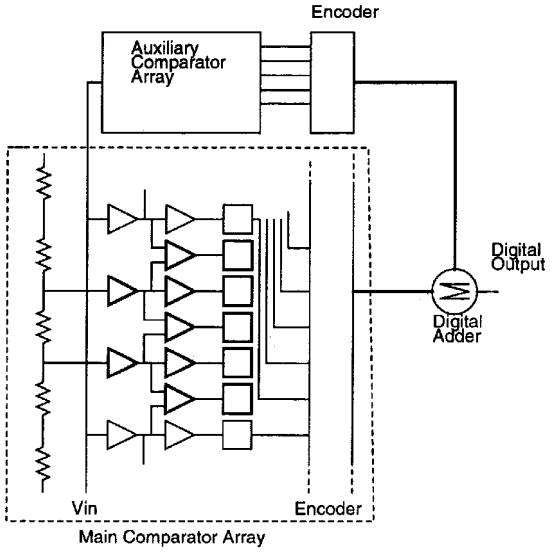

Fig. 7. Configuration during the second part of an aurozero cycle

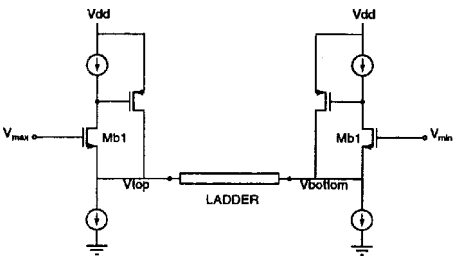

Fig. 8. Reference pre-distortion circuit

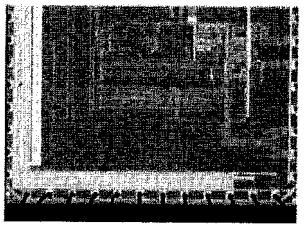

Fig. 9. microphotograph of the A/D converter

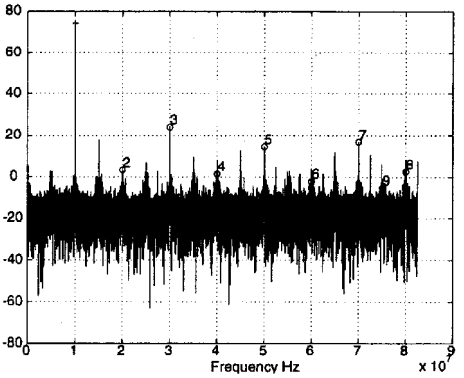

Fig. 10. Output spectrum for fin = 10 MHz and fs = 165 Msamples/s

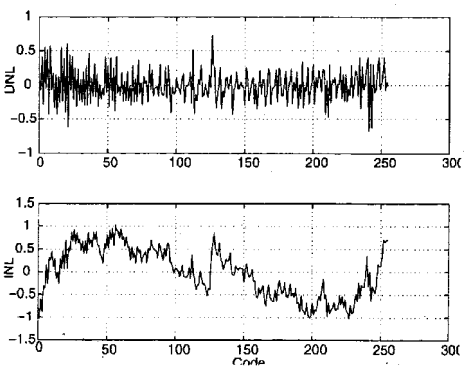

Fig. 11. Measured DNL and INL with fs = 165 Msamples/s