WP 26.1 A 700MSample/s 6b Read Channel A/D Converter with 7b Servo Mode

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This 6b CMOS analog to digital converter (ADC) for hard disk drive (HDD) applications has a 7b mode for servo signal processing. The top level block schematic of the ADC is shown in Figure 26.1.1. The input is sampled and held by the sample and hold (S/H) circuit. The output of the S/H is processed by a circuit called the 7b interface which enables operation of the 7b mode. In the 6b mode this circuit acts as a short. The output from this circuit is fed into the comparator array which converts the input signal into a digital thermometer code which is converted to a 1 of 64 code by the bubble correction logic. This in turn is fed into a ROM type encoder that generates the final 6b digital output.

The S/H circuit employs a pseudo-differential architecture made up of two single-ended circuits. The block schematic of one single-ended path is shown in Figure 26.1.2. An important feature of this architecture is that it uses two inter-leaved S/H circuits operating at half the sampling frequency. The inter-leaving has two advantages. First, the acquisition time available for each S/H is twice that which would be available if a single S/H circuit were used. Second, the final output of the S/H is held for an entire clock interval. This dramatically eases the design of the output buffer that drives the comparator array.

Details of one inter-leaved path in the S/H are shown in Figure 26.1.3. The source follower M3 constitutes the input buffer and the source follower M5 constitutes the final output buffer. These are common to the two inter-leaved paths. The core S/H circuit consists of the sampling switch M1, hold capacitor C1, and the source follower M4. To minimize intermodulation distortion due to mismatches between the two inter-leaved sampling clocks, the circuit of Figure 26.1.3 synchronizes the two inter-leaved paths with the master clock (CLK). This is achieved by the switches connected to the gate of M1. The clock signal ph2q goes high a short time before CLK goes high, whereas ph2 goes high a short time after CLK goes high. Thus, as soon as CLK goes high the gate of M1 is pulled low, causing the S/H to go into the hold mode. It continues to be in the hold mode until ph2 goes low. The other inter-leaved path has a similar arrangement.

Two measures are taken to achieve the required level of distortion [1]. First, the gate voltage of the sampling switch during the tracking mode is made equal to Vin + Vb by using a switched-capacitor boot-strap circuit consisting of capacitor C2 and associated switches in Figure 26.1.3. This ensures that the gate overdrive is independent of the input level, minimizing distortion due to signal-dependent switch feedthrough. Signal-dependent feedthrough from the gate to drain capacitance of M1 is minimized by using an identical dummy transistor M2 which is always turned off. When the S/H goes from the tracking mode to the hold mode, the gate of M2 is switched from ground to the output of the S/H. Thus the gate drain capacitances of M1 and M2 experience equal and opposite transitions, cancelling their feed-through.

The overall comparator array structure is shown in Figure 26.1.1. The analog signal path is fully differential. Each comparator consists of first stage preamp (P1), second stage preamp (P2), and latch. To reduce comparator input capacitance and to save area, interpolation is used to eliminate half of the first stage preamps. If the preamps have large offsets, the DNL of the ADC degrades. Common techniques for overcoming such offsets include large input transistors and special autozero cycles [2]. In this ADC, the preamp offsets are cancelled during a special autozero (AZ) period, which lasts approximately 50ns and takes place during idle intervals that occur periodically (every 100µs or so) in a HDD read channel. During the first part of the AZ period, P1 is reset so the input of P2 is zero, and P2 is autozeroed. For the interpolated P2s, this also cancels any offset due to differences in the P1 common mode outputs. P2 offset is stored on grounded capacitors inside P2. P1 is autozeroed during the second part of the AZ period. The reference levels and and the offsets of P1 are stored on the coupling capacitors (C+,C-).

The schematic for P1 is shown in Figure 26.1.4. P2 is essentially the same except that it has four inputs (using two differential pairs) instead of two inputs. M5 and M6 serve as current source load transistors while M3 and M4 serve as the input transconductors. During the first half of every clock cycle, the preamp is reset by the reset switch; the preamp performs the amplification during the second half of the clock cycle. M1 and M2 serve two purposes. First, they form the tail current source for M3 and M4. Second, since their gates are tied to the outputs, they provide common-mode feedback.

Seven-bit resolution is required in a read channel for processing servo data. Taking advantage of the lower rate of the servo data, 7b operation is achieved using a two step technique that requires little extra circuitry, as illustrated in Figure 26.1.5 [3]. A 6b A/D conversion is first performed with an analog voltage equal to 1/2 LSB added to the output of the S/H. The LSB (b1 in Figure 26.1.5) from this operation is stored in a 1b memory element D. During the second step, a 6b A/D conversion is performed without the 1/2 LSB added to the input. If the input were to lie in the upper half of a 6b LSB interval, adding the 1/2 LSB would push the result of the conversion into the next higher digital code. Thus, the results from the first and second steps would be different. This condition, detected with an exclusive-OR operation, determines the 7th bit.

The addition of the 1/2 LSB offset is achieved by using a small resistor (equal to one half of an element in the reference ladder) in series with the S/H output and applying a current (equal to the current in the reference ladder) to it. Note that during both steps the current Iref ultimately flows into the the output buffer in the S/H circuit. This is important to ensure that there is no change in the S/H output itself between the two steps.

The ADC is fabricated in 0.25µm single-poly four-level-metal CMOS. In the 6b mode, at 700MSamples/s, with 3.3V and 1.8V supplies, the ADC consumes 187mW. Figure 26.1.6 shows the FFT of the ADC output in the 6b mode; the SNDR is 35.2dB for Fin=136MHz, Fs=700MSamples/s. At Fin=247MHz, Fs=500MSample/s, and Vin=0.6 of fullscale, the measured SNDR is 31.8dB. Measured INL and DNL for the 6b mode are shown in Figure 26.1.7. The measured intermodulation distortion due to the inter-leaving is 55dB below the fundamental. Measured performance is summarized in Figure 26.1.8. Figure 26.1.9 shows a chip micrograph.

Acknowledgments:
The authors acknowledge contributions from M. Chambers, M. Barnett, K. Kistner, A. Brewster, V. Pierotti, M. Spaeth, B. Liebowitz, and M. Peng.

References:
[1] Nagaraj, K., F. Chen, T. Lo and T.R. Viswanathan, "Efficient 6b A/D Converter using a 1b Folding Front End", IEEE Journal of Solid State Circuits, Vol. 34, pp 1056-61, August 1999.
[2] Yuko, T. and Yamakido, K., "A CMOS 6b 500MSample/s ADC for a Hard Disk Drive Read Channel", ISSCC Digest of Technical Papers, pp.324-325, February, 1999.
[3] Nagaraj, K., "2 1/2 Step Flash A/D Converter", Electronics Letters, October 1992.

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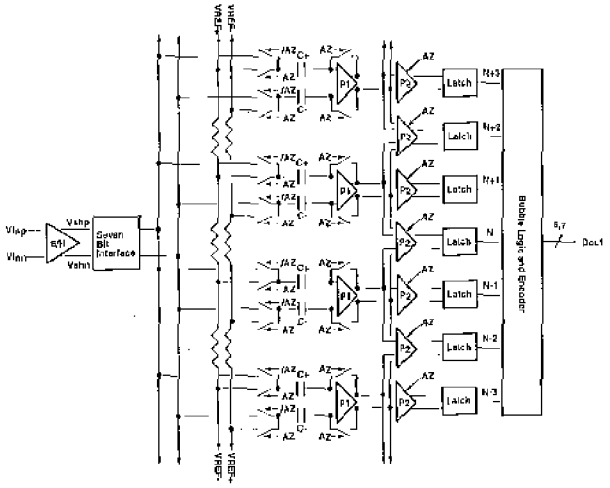

Figure 26.1.1: ADC block diagram, showing part of the comparator array.

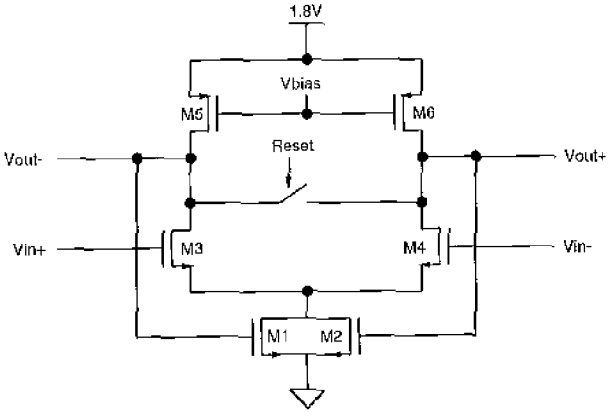

Figure 26.1.4: First stage preamp schematic.

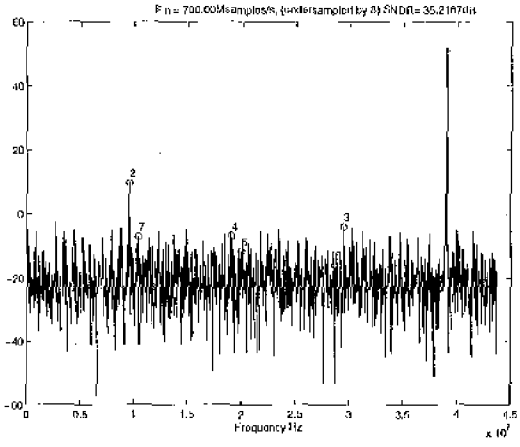

Figure 26.1.6: SNDR plot, 6b mode, Fin=136MHz.

Figure 26.1.7: See page 476.

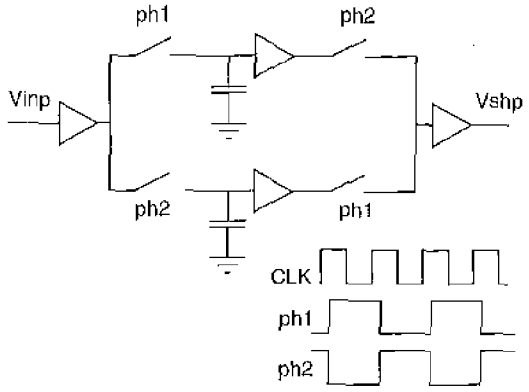

Figure 26.1.2: S/H half circuit of a single-ended path.

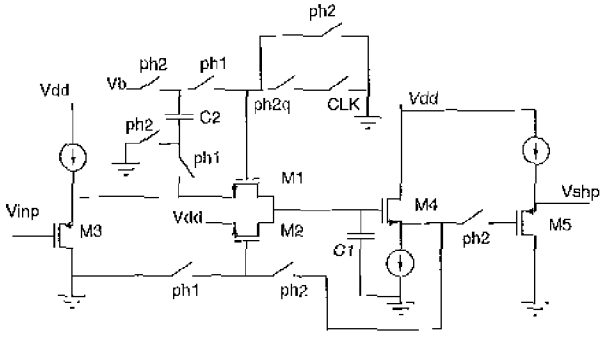

Figure 26.1.3: An inter-leaved path in the S/H.

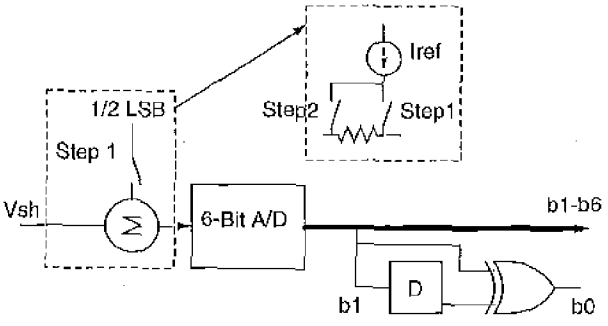

Figure 26.1.5: Principle of 7b mode operation.

CMOS technology	1poly, 4metal, 0.25μm	
Supply voltages	3.3V, 1.8V	
Input range	1.0V p-p	
ADC area	0.45mm²	
Resolution	6b	7b
Conversion rate	700Msample/s	200Msample/s
Power consumption	187mW	143mW
DNL	<0.4LSB	<0.4LSB
INL	<0.4LSB	<1.0LSB
SNDR	35.2dB	41dB
F_{in} for SNDR measurement	136MHz	53MHz
Tone at $F_s/2\pm F_{in}$	-55dB with F_{in}=136MHz, F_s=600Msample/s	

Figure 26.1.8: ADC performance summary.

Figure 26.1.9: See page 476.

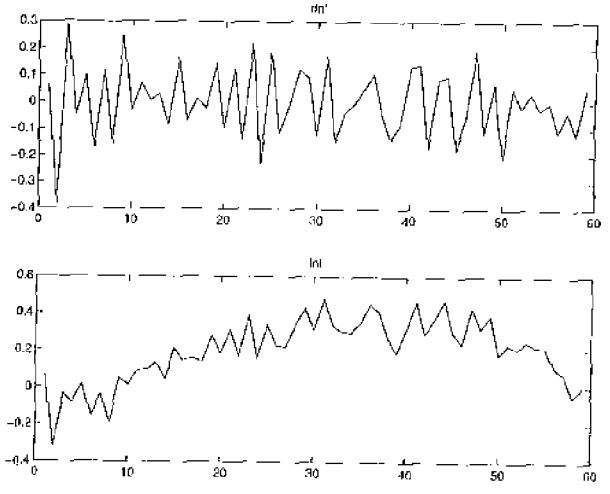

Figure 26.1.7: DNL and INL, Fin=23MHz, Fs=700MSample/s.

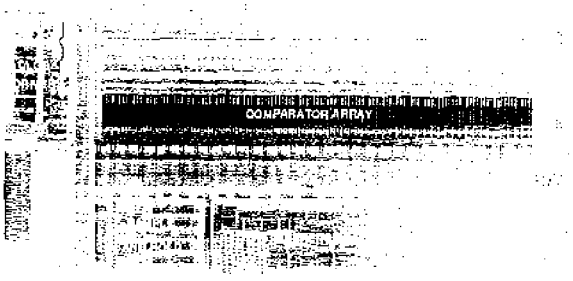

Figure 26.1.9: ADC micrograph.

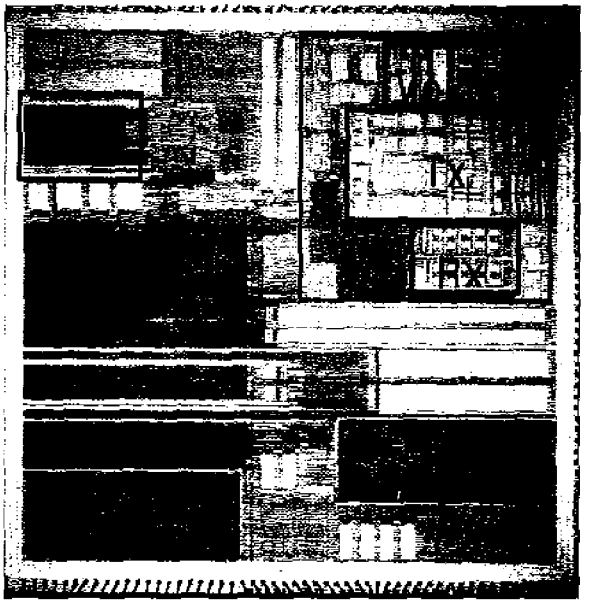

Figure 26.5.5: Chip micrograph.

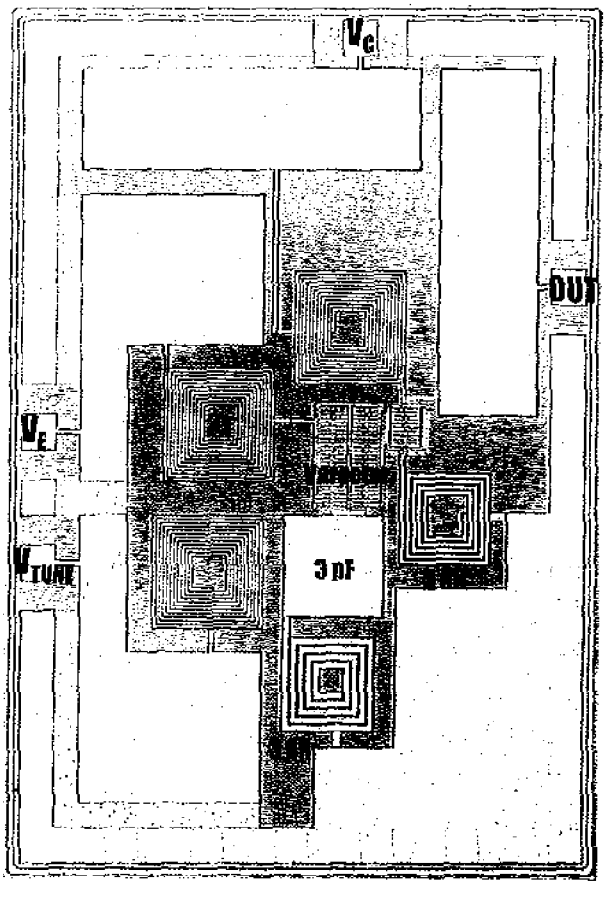

Figure 26.4.7: Die micrograph.

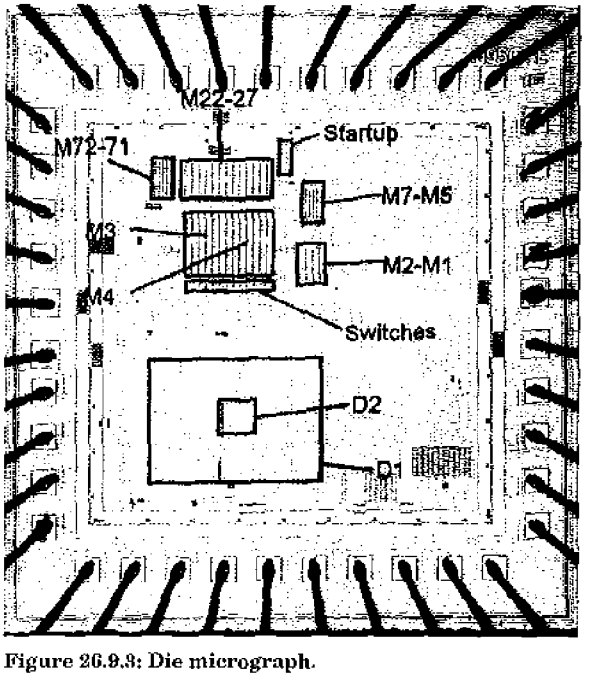

Figure 26.9.3: Die micrograph.

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