A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS Process

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***Abstract*—The design of a high-speed analog-to-digital (A/D) converter for hard disk drive read channels is described. The A/D converter uses a flash architecture with an interleaved sample and hold and interpolating comparator pre-amplifiers. It has 6 bits of resolution at full speed as well as a 7-bit mode operating at a lower speed. The 7-bit mode is useful for servo signal processing. This A/D converter has been implemented in a four-level metal single-poly 0.25-μm CMOS technology. The device operates at a speed of up to 700 MSamples/s in the 6-bit mode while maintaining an signal-to-noise-plus-distortion rate (SNDR) of greater than 35 dB at input frequencies of up to one-fourth the sampling rate. In the 7-bit mode, the device operates at up to 200 MSamples/s with a SNDR greater than 41 dB. It occupies an active area of 0.45 mm^2 and consumes less than 187 mW of power.**

***Index Terms*—A/D converters, CMOS analog integrated circuits, data converters.**

I. Introduction

VERY HIGH-SPEED medium-resolution analog-to-digital (A/D) converters are an essential part of modern data communication receivers and hard disk drive read channels [1]–[8]. With the trend toward the integration of larger systems, it is important to realize such A/D converters in digital CMOS technologies. Area and power consumption are also important considerations in these applications.

This paper describes a 6-bit CMOS A/D converter that has been designed for hard disk drive read channel applications. The design has been carefully optimized by taking into account system considerations. The prototype exhibits 6-bit performance at a sampling frequency of up to 700 MSamples/s. The converter also has a 7-bit mode working at up to 200 MSamples/s. This mode is useful for servo signal processing, which is essential for determining the position of the read head over the rotating disk.

The A/D converter uses a flash architecture. The S/H uses interleaving to achieve the necessary speed and a constant VGS sampling switch to reduce distortion. The comparator pre-amplifiers use interpolation to reduce area and power and an integrating architecture to minimize power as well as to increase dc gain. The comparators are auto-zeroed frequently during the A/D converter's idle periods. The A/D converter also has a 7-bit mode at half the speed.

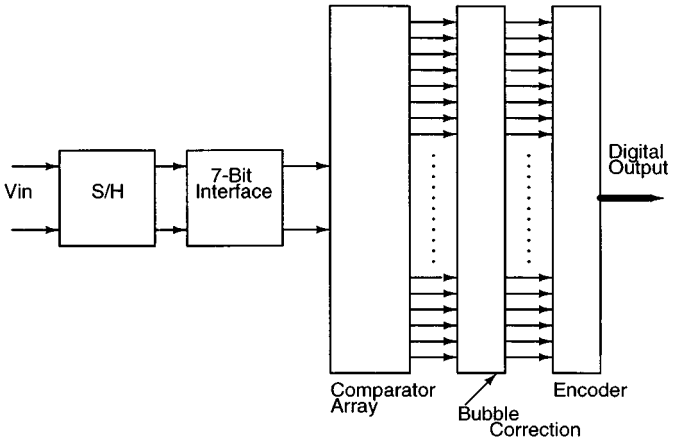

Fig. 1. Block schematic of the A/D converter.

The top-level block schematic of the converter is shown in Fig. 1. The input is sampled and held by the sample and hold (S/H) circuit. The S/H is described in Section II. The output of the S/H is processed by a circuit block called the 7-bit interface which facilitates the operation of the 7-bit mode. The operation of this circuit is described in Section V. In the 6-bit mode, the 7-bit interface behaves like a short circuit. The output from this circuit is fed into the comparator array that converts the input signal into a digital thermometer code. This digital output is connected to a bubble correction logic that converts the thermometer code into a 1 of 64 code. This in turn is fed into a ROM-type encoder that generates the final 6-bit digital output. The comparator and digital logic are described in Section III. The reference circuit is described in Section IV. Finally, the experimental results are presented in Section VI.

II. Sample and Hold Circuit

The S/H circuit employs a pseudodifferential architecture made up of two single-ended S/H circuits, as shown in Fig. 2. The block schematic of each single-ended S/H circuit is shown in Fig. 3. An important feature of this architecture is that it uses two interleaved track and hold (T/H) circuits operating at half the sampling frequency. These are used in a time-interleaved manner to achieve one S/H function. The input signal is first buffered by Buf1 before being fed into the two interleaved

Manuscript received April 15, 2000; revised June 27, 2000.

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Publisher Item Identifier S 0018-9200(00)10051-4.

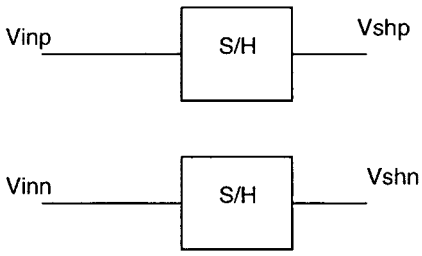

Fig. 2. Block schematic of the S/H circuit.

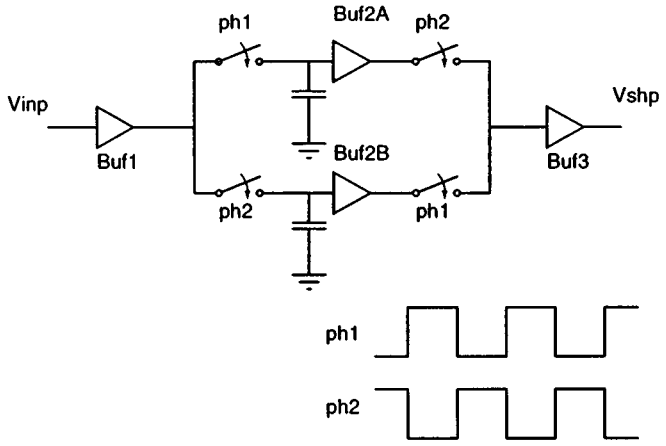

Fig. 3. Block schematic of one single-ended S/H circuit path.

paths. The input buffer is needed due to the low drive capability of the preceding circuit in this application. Each of these paths consists of a sampling switch which is followed by the buffer Buf2A or Buf2B. The two interleaved outputs are recombined using a set of pass gates. The recombined signal is fed into a common output buffer Buf3 that drives the comparator array. The interleaving has two advantages. First, the acquisition time available for each T/H is twice that which would be available if a single S/H circuit was used. This makes the design of the T/H circuit more manageable. A second important advantage of interleaving is that the final output of the S/H is a 'held' signal for an entire clock interval. This dramatically eases the design of the output buffer that drives the comparator array.

The details of one interleaved path are shown in Fig. 4. The source follower M3 constitutes the input buffer Buf1 of Fig. 3 and the source follower M5 constitutes the final output buffer Buf3 of Fig. 3. These are common to the two interleaved paths. The core T/H circuit consists of the sampling switch M1, the hold capacitor C1, and the source follower M4, which constitutes the internal buffer Buf2A or Buf2B of Fig. 3 for the core T/H. Several measures have been taken in this circuit to achieve the required level of performance. First, a constant voltage is applied between the gate and source of M1 during the tracking mode. This ensures that the gate overdrive is independent of the input level, thus eliminating distortion due to signal dependent switch feedthrough. Another source of signal-dependent feedthrough is the gate–drain capacitance of M1. This is minimized by using the dummy transistor M2 which is identical to M1. When the T/H goes from the tracking mode to the hold mode, the gate of M2 is switched from ground to the output of

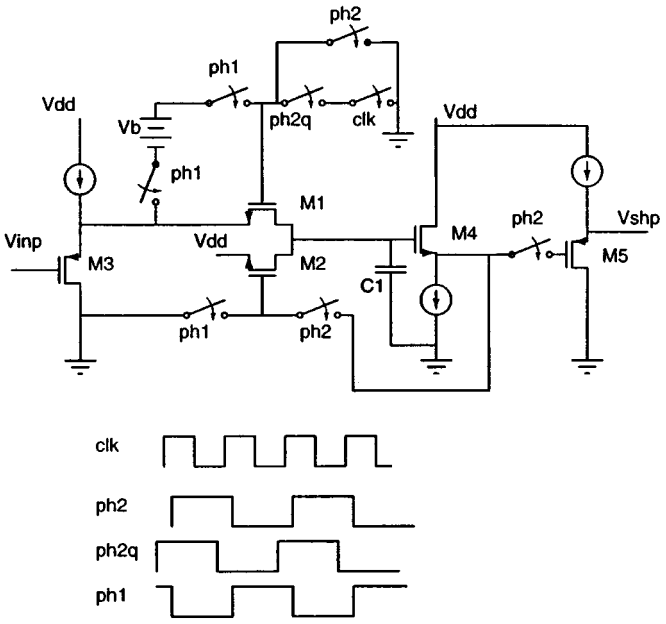

Fig. 4. Circuit schematic of an interleaved path in a T/H.

the T/H. Thus the gate–drain capacitances of M1 and M2 experience equal and opposite transitions, canceling their feedthrough. Note that M2 is always turned off.

A potential problem with interleaving is the mismatch between the two channels. There are three possible sources of mismatch. Any timing mismatch or gain mismatch results in an intermodulation between the input frequency and half the sampling frequency. Any offset mismatch results in a tone at half the sampling frequency. This is not a problem in a read channel application because this tone is suppressed by the digital equalizer that follows the A/D converter. Timing mismatch is the most serious among these sources of mismatch. To minimize the effect of this mismatch, the circuit of Fig. 4 synchronizes the two interleaved paths with the master clock. This is achieved by means of the switches connected to the gate of M1. The clock signal *ph2q* goes high a little before *clk* goes high, whereas *ph2* goes high a little after *clk* goes high. Thus, as soon as *clk* goes high the gate of M1 is pulled low, causing the S/H to go into the hold mode. When *ph2* goes high it shorts the gate of M1 to ground through a parallel switch. This ensures that the T/H continues to be in the hold mode until *ph2* goes low. The other interleaved path has the same arrangement except that *ph2* and *ph2q* are replaced by *ph1* and *ph1q*. The instant at which either of the interleaved paths goes into the hold mode is synchronized to the rising edge of *clk*, eliminating the error due to any mismatches between *ph1* and *ph2*. This elimination of timing mismatch was sufficient for this 6-bit A/D converter. The gain and offset mismatch of the interleaved T/Hs were small enough for the A/D converter as well.

The constant gate overdrive for M1 is achieved by using a switched-capacitor arrangement, as shown in Fig. 5. Here the capacitor C2 is charged to the voltage V_b during the hold phase (*ph2* in Fig. 3). During the tracking phase *ph1*, the bottom plate of C2 is connected to the input voltage whereas the top plate is connected to the gate of M1. Thus, the gate-to-source voltage of

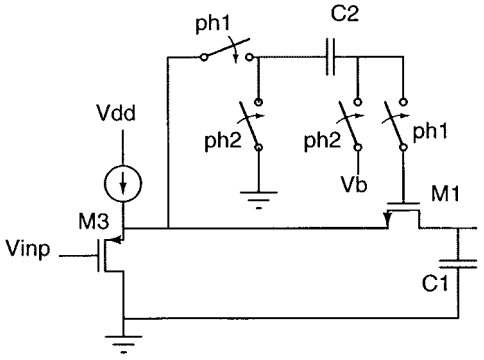

Fig. 5. Details of the sampling switch showing the generation of the constant gate overdrive.

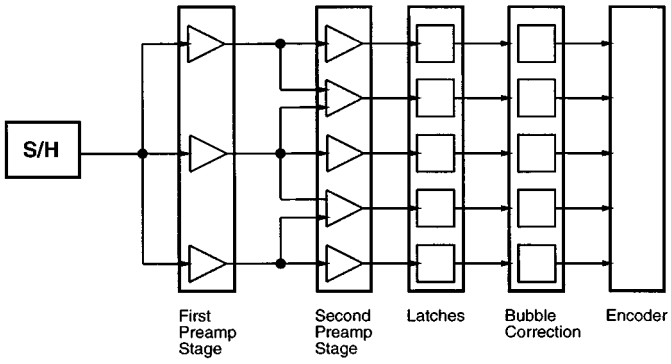

Fig. 6. Overall comparator structure.

M1 during the tracking mode is constant [9], [10]. The voltage V_b is derived from the analog supply voltage by means of a simple potential divider.

III. Comparator Design

The overall structure of the comparator array is shown in Fig. 6. The comparator array refers to all of the circuitry in Fig. 6 except the S/H circuit and encoder. Although not shown in the figure, the analog signal is differential.

The output of the S/H circuit is compared against 2^N differential references, the differences are amplified by the preamps and then latched by the latches. The latches take the analog input (now amplified by the preamps) and convert them to ones or zeroes. The bubble correction logic eliminates some types of bubbles and converts the thermometer code into a '1-of-64' code. The encoder then encodes this to a 6-bit output.

To reduce the input capacitance of the comparators and to save area and power, the preamps use interpolation to eliminate half of the first stage of preamps.

The offset voltages of the preamps are cancelled during a special autozero period. This period lasts approximately 50 ns and takes place during idle times that periodically occur (approximately every 100 μs) in a hard disk drive read channel.

A. First-Stage Preamp

The operation of the first-stage preamp P1 is shown in Fig. 7. During an autozero period, the reference voltages, produced by a resistor ladder, are connected to one side of the input capacitors while feedback loops are connected around the preamp. Because of interpolation, only 2^{N-1} rather than 2^N differential reference voltages are needed. For conversion cycles, the feedback around the preamp is opened, and the capacitors are connected to the S/H output instead of the resistor ladder. The voltage stored on the capacitors is equal to the reference voltage minus the preamp's common-mode voltage. Note that this scheme also cancels the offsets of the first-stage preamp since the offset voltage is also stored on the capacitors. The scheme does not reduce any offets due to mismatch in the resistor ladder. For six bits of resolution, this is not a problem.

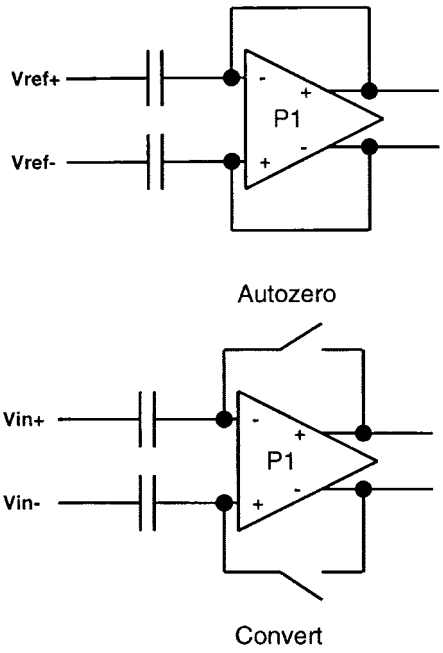

Fig. 7. First-stage preamp operation.

The schematic for P1 is shown in Fig. 8. The reset switch is an nMOS transistor. M3 and M4 constitute the input differential pair, while M5 and M6 serve as constant current loads. M1 and M2 serve two purposes. First, they form the tail-current source for M3 and M4. Second, since the gates of M1 and M2 are tied to the outputs, they provide the common-mode feedback. If the output common mode goes up, the common mode of the gates of M1 and M2 goes up, which causes more current to flow, which tends to bring the output common mode down. The preamp is reset during one half of every clock cycle by turning on the reset switch. As soon as the reset goes low, the amplifier simply 'integrates' the input and the output grows until the end of the clock cycle. This integrating behavior results from the fact that the amplifier has a large output impedance. This is in contrast to amplifying type preamps, which settle to a certain multiple of their input, that have been used in other high-speed A/D converters [7]. The integrating type preamp used above requires a smaller amount of power to achieve the desired dynamic gain. It also has a larger dc gain that enables better offset cancellation.

B. Second-Stage Preamp

The operation of the second-stage preamp (P2) is shown in Fig. 9. P2 is autozeroed at the same time as P1. To make sure that the differential input of P2 is zero during autozero, P1 is

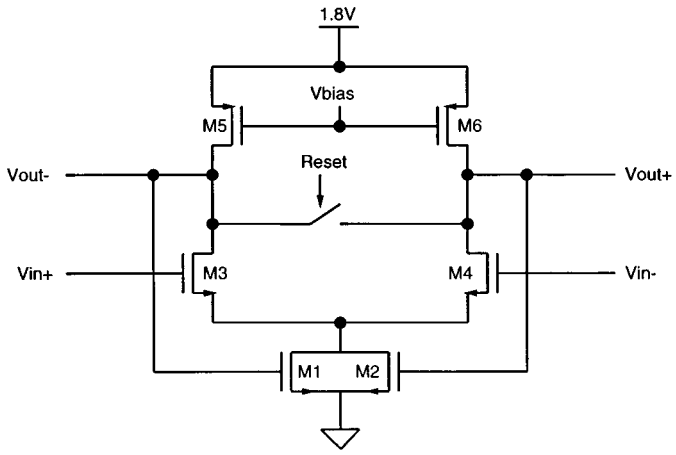

Fig. 8. Circuit schematic of the first-stage preamp.

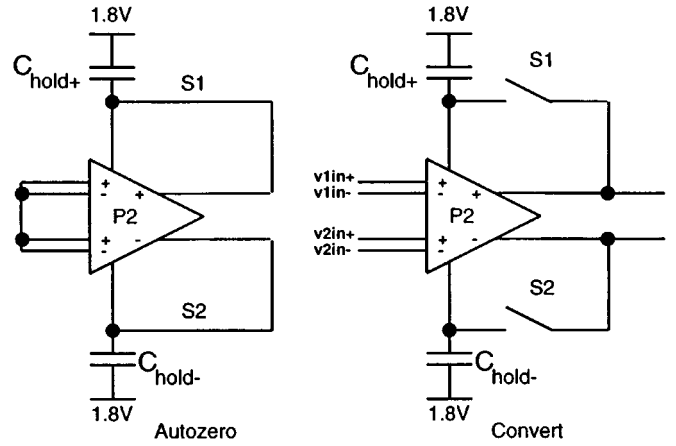

Fig. 9. Second-stage preamp operation.

reset during that period. During this autozero, the outputs of P2 are looped back to auxiliary inputs so that the differential output is approximately equal to the offset of P2 referred to the auxiliary input. This voltage is stored on the capacitors $C_{\text{hold}+}$ and $C_{\text{hold}-}$.

The schematic for P2 is shown in Fig. 10. M1–M2 and M3–M4 serve as the two input differential pairs, while M5 and M6 serve as current-source loads. M11 and M12 constitute the auxiliary input pair for offset cancellation. M7, M8, M9, and M10 serve the same purpose as M1 and M2 in the first-stage preamp. P2 integrates its input in the same way as P1.

M14 and M15 serve as hold capacitors for the gate voltages of M12 and M11. This is the C_{hold} of Fig. 9 where the offset of the preamp is stored. The switches S1 and S2 connect the outputs to the gates of M12 and M11. This feedback around the differential pair then acts to cancel the preamp's offset [11]. S1 and S2 are formed using nMOS transistors.

Because of the interpolation used for the preamps, P2 may have inputs from two different first-stage preamps; thus, it has two sets of differential inputs and thus four input transistors. The drains of the input transistors are connected so that the positive inputs steer current into one leg of the preamp, and the negative inputs into the other leg. Note that the input transistors have two different current sources rather than one. The reason for this is that it is possible that two first-stage preamps might have slightly different common-mode output voltages due to mismatches. If the second-stage preamp's input transistors all shared the same current source, then the two input transistors connected to the first-stage preamp with the higher common-mode output voltage would tend to use more current than the other two input transistors. In that case, the second-stage preamp would no longer be performing an exact interpolation between the two first-stage preamps. Rather, one first-stage preamp would dominate the result. This problem is avoided by using two current sources for the input transistors of the second-stage preamp. It is important that the two current sources match each other. For six bits of resolution, this is not a problem.

The timing diagram for the operation of the pre-amplifiers during conversion is shown in Fig. 11.

C. Autozero Timing

For proper offset cancellation, the autozero controls to the two preamplifiers need to follow a particular sequence. The clock signals for an autozero are shown in Fig. 12. First, *AZ*, *CANCEL*1, and *CANCEL*2 all go high. During the first part of the autozero cycle (when *CANCEL*2 is high) the second-stage preamps cancel their offset. Then, halfway through an autozero cycle, *CANCEL*2 goes low, and then *P*1*RESET* goes low. This removes the reset on the first-stage preamps and allows them to autozero themselves. When this is completed, *CANCEL*1 goes low. Finally, *AZ* goes low, and conversion cycles can begin.

The autozero cycle lasts approximately 50 ns and takes place approximately every 100 μs.

D. Latch Circuit

The latch circuit comprises of a primary latch followed by a flip-flop. The flip-flop reduces metastability by adding another clock delay to the time needed for the signal to settle to a valid digital level.

The schematic of the primary latch is shown in Fig. 13. It consists of two cross-coupled inverters whose power supplies are turned on or off by a *STROBE* signal, shown as S in Fig. 13. During the clock phase when the pre-amplifiers are amplifying, the latch is connected to the preamp outputs by means of pass gates. The latch offset can be overcome by an input voltage of at least LSB$/4$ when amplified by the preamps. During the next clock phase the latch is disconnected from the pre-amplifier and the *STROBE* is turned on, initiating the latching action. The latch is then reset by shorting its outputs together before being connected to the preamp again.

E. Bubble Logic

The bubble logic which converts the thermometer-coded latch outputs into a 1-of-64 code is shown in Fig. 14. It also eliminates single-bit boundary and single-bit deep bubbles in the thermometer code. $D_{(n)}$ is the digital output of comparator n. $D_{out(n)}$ goes to the encoder.

CKDIG is high during the first part of a clock cycle. While *CKDIG* is high, $D_{out(n)}$ goes low. When *CKDIG* goes low,

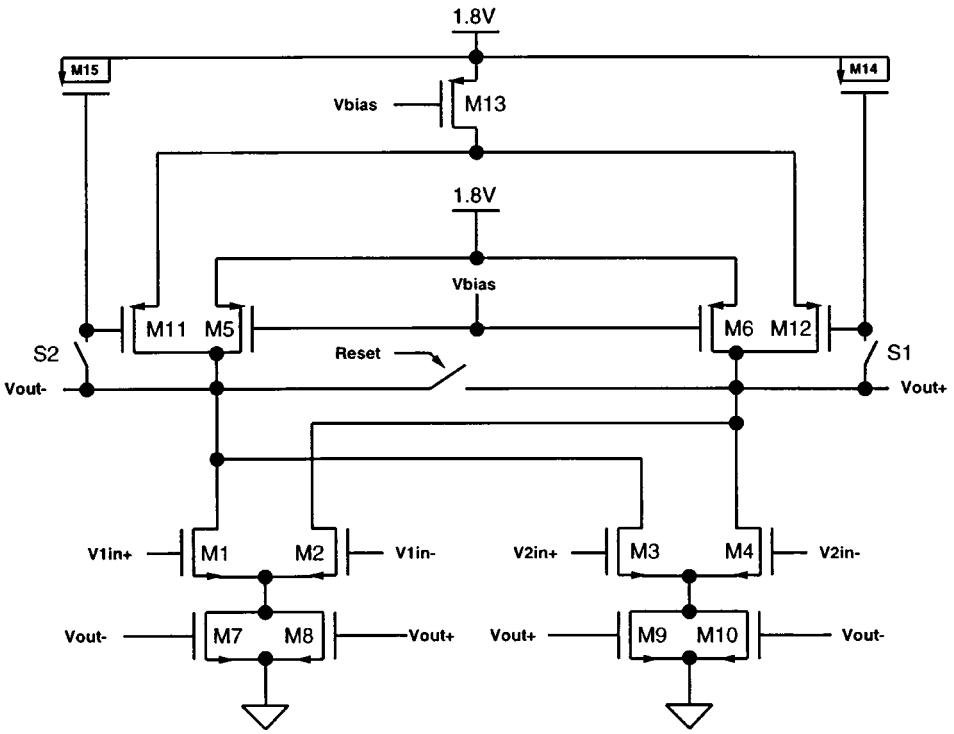

Fig. 10. Circuit schematic of the second-stage preamp.

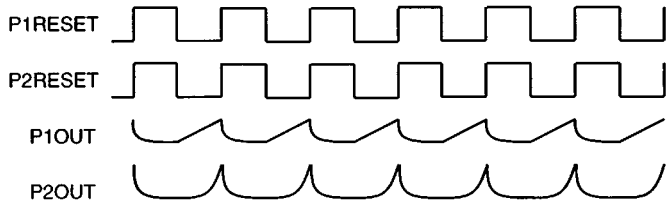

Fig. 11. Timing diagram of the operation of the pre-amplifiers.

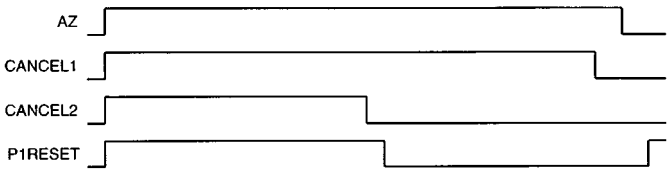

Fig. 12. Timing diagram for an autozero operation.

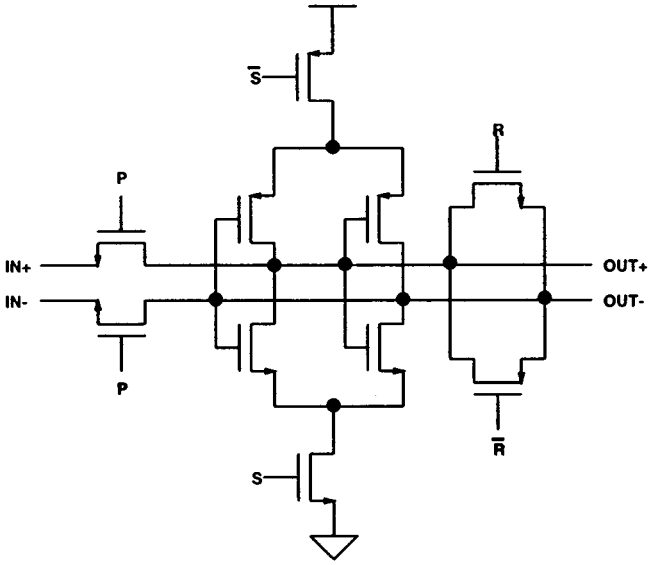

Fig. 13. Circuit schematic of the primary latch.

$D_{out(n)}$ will go high only if two of $D_{(n-1)}$, $D_{(n)}$, and $D_{(n+1)}$ are high, and two of $D_{(n)}$, $D_{(n+1)}$, and $D_{(n+2)}$ are low [12].

IV. Reference Generator

A block schematic for the reference-voltage generator for the comparator array is shown in Fig. 15. It receives two inputs: a bandgap-referenced voltage $V_{\rm BG}$ and an input common-mode reference voltage $V_{\rm cmi}$. The function of the reference generator is to impose the reference voltages $V_{\rm refp}$ and $V_{\rm refn}$ across the two resistor ladders such that the difference between $V_{\rm refp}$ and $V_{\rm refn}$ equals half the required full scale reference voltage, and their common-mode level is equal to the common-mode output level of the S/H circuit. This common-mode level is dependent on the gate-source voltage drops of the source followers in the S/H, and is thus process and temperature dependent. To overcome this problem, the reference generator uses the replica circuit SHREF that accepts $V_{\rm cmi}$ as an input and generates a signal $V_{\rm cmr}$, which is equal to the common-mode level of the S/H output. The circuit SHREF consists of three source followers that are scaled versions of those in the main S/H circuit. From $V_{\rm cmr}$, the voltage $V_{\rm refp}$ is derived by means of the amplifier A2 and resistor R2. By setting R2 equal to half the total resistance of the ladder, we can ensure that $V_{\rm refp} = V_{\rm cmr} + ((I_{\rm ref})(R2)/2)$, which is the correct value required at the top of the resistor ladder. This voltage is applied to the top of the ladder. Simultaneously, a current sink

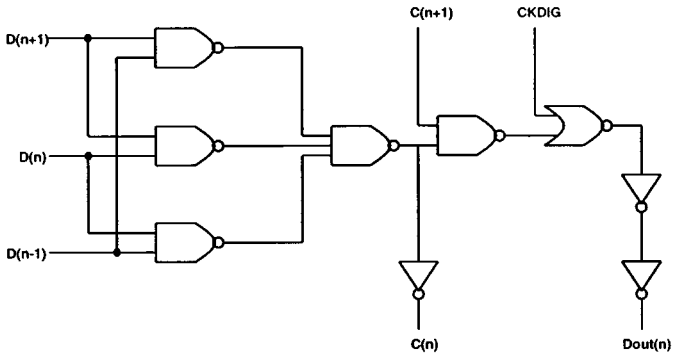

Fig. 14. Circuit schematic of the bubble logic.

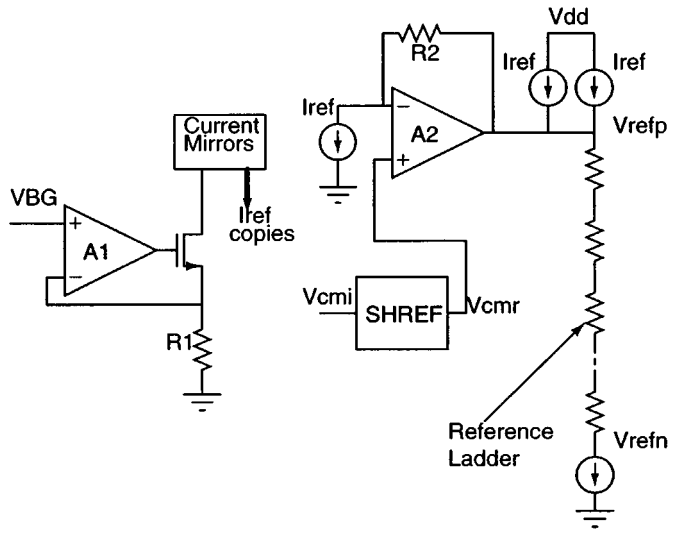

Fig. 15. Block schematic of the reference generator.

equal to $I_{\rm ref}$ is attached to the bottom of the ladder. This ensures that voltage across the ladder has the correct value. Note that two current sources equal to $I_{\rm ref}$ are connected to the top of the resistor ladder. Thus, the amplifier A2 is not required to sink or source any significant amount of current. The current $I_{\rm ref}$ is derived from $V_{\rm ref}$ using a V–I converter made up of A1 and R1. The current output from this circuit is fed into a current mirror that generates the current sources and sinks that are required by the other parts of the reference generator. Because they have a long time to settle, the bandwidth requirements of A1 and A2 are very low.

V. Operation of the 7-Bit Mode

Servo signal processing in a read channel requires a higher resolution than that required for processing normal data. One method of obtaining an extra bit of resolution is to use an additional set of interpolating latches to generate the seventh bit [8], [13], but this requires a significant amount of extra circuitry. An alternative area-efficient approach is to use a two-step architecture, taking advantage of the fact that the servo data rate is slower than the normal data rate. In conventional two-step architectures [13], [14], the decision bits from the first step are required for the second step. This becomes a serious problem at high speeds. In this A/D converter, 7-bit operation is achieved using a modified two-step approach that does not have this problem [15].

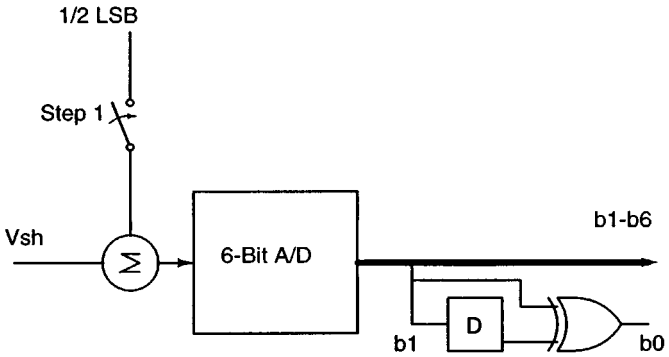

Fig. 16. Principle of operation of the 7-bit mode.

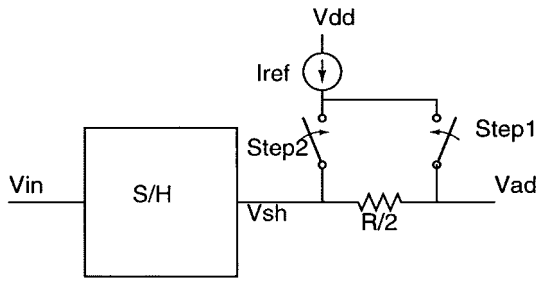

Fig. 17. Circuit schematic of the analog 1/2 LSB adder.

The principle of operation of the 7-bit mode is illustrated in Fig. 16. During the first step, a 6-bit A/D conversion is performed with an analog voltage equal to 1/2 LSB at the 6-bit level added to the output of the S/H. The LSB (b1 in Fig. 16) from this operation is stored in a 1-bit memory element D. During the second step, a 6-bit A/D conversion is performed without the 1/2 LSB added to the input. If the input were to lie in the upper half of a 6-bit LSB interval, adding the 1/2 LSB would push the result of the conversion into the next higher digital code. Thus, the results from the first and second steps would be different. This condition is detected by means of an exclusive-OR operation between the sixth bits from the two steps. The output of the exclusive-OR gate gives the seventh bit. The important feature here is that the digital bits from the first step are not required to perform the second step, in contrast to conventional two step architectures.

The addition of the 1/2 LSB voltage is achieved by the 7-bit interface circuit shown in Fig. 17 (a single-ended equivalent is shown; the actual circuit is differential). A resistor equal to one-half of each element in the ladder is inserted in series with the S/H output. A current $I_{\rm ref}$ equal to the current in the reference ladder is applied to this resistor during the first step, resulting in the required 1/2 LSB offset. Note that during both the steps the current outputs ultimately flow into the output buffer of the S/H circuit. This ensures that the output of the S/H itself does not change from the first step to the second.

Note that to do a 7-bit conversion at X MHz, the circuit must be clocked at $2X$ MHz in order to perform the two 6-bit conversions.

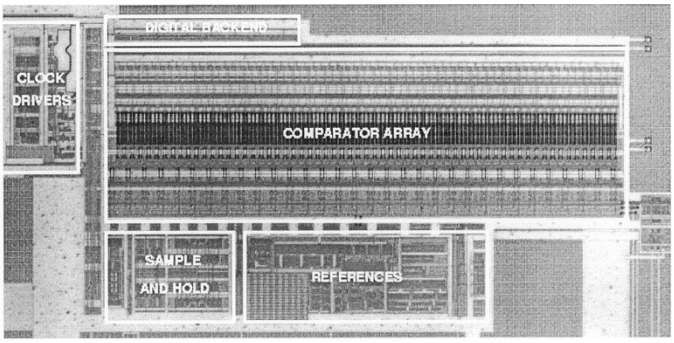

Fig. 18. Photomicrograph of the A/D coverter.

TABLE I
A/D CONVERTER PERFORMANCE SUMMARY

CMOS Technology	1-poly, 4-metal, .25μm	
Supply Voltages	3.3V, 1.8V	
Input Range	1.0V p-p	
A/D Converter Area	.45 mm^2	
Resolution	6-bit	7-bit
Conversion Rate	700 Msamples/s	200 Msamples/s
Power Consumption	187mW	143mW
DNL	< 0.4 LSB	< 0.4 LSB
INL	< 0.4 LSB	< 1.0 LSB
SNDR	35.2dB	41dB
Fin for SNDR measurement	136MHz	53MHz
Tone at Fin +/− Fs/2	-55 dB at Fin=136 MHz, Fs=600 MHz	

A. Output Interface

Driving the digital outputs is a problem in very high-speed A/D converters because of the large currents required to charge and discharge the load capacitances. This can lead to a large bounce on the supply and ground leads. To minimize this, current steering type output buffers have been used in this device.

Further, the logic analyzer used to collect the A/D converter's digital output could not collect data above 100 MHz, so it was necessary to undersample the digital output. This was controlled by an external clock that could be a submultiple of the main clock. By a proper choice of the relationship between the input frequency and the main clock frequency, we can obtain the necessary spectral information even from such undersampled outputs.

VI. EXPERIMENTAL RESULTS

The A/D converter was fabricated in a four-level metal single-poly 0.25-μm digital CMOS process. A photomicrograph of the chip is shown in Fig. 18. Measured performance is summarized in Table I.

In the 6-bit mode, at 700 MSamples/s, with 3.3 and 1.8-V supplies, the A/D converter consumes 187 mW of power. The 3.3-V supply is used by the S/H circuit and by the reference block. The rest of the A/D converter uses the 1.8-V supply. Fig. 19 shows the output spectrum of the A/D converter output in the 6-bit mode; the SNDR is 35.2 dB for $F_{in} = 136$ MHz, $F_s = 700$ MSamples/s. The large second harmonic seen in the spectrum is a result of the single-to-differential conversion circuit in the test setup. At $F_{in} = 247$ MHz, $F_s = 500$ MSamples/s, and $V_{in} = 0.6$ of full-scale, the measured SNDR is 31.8 dB. Measured differential nonlinearity (DNL) and integral nonlinearity (INL) for the 6-bit mode are shown in Fig. 20.

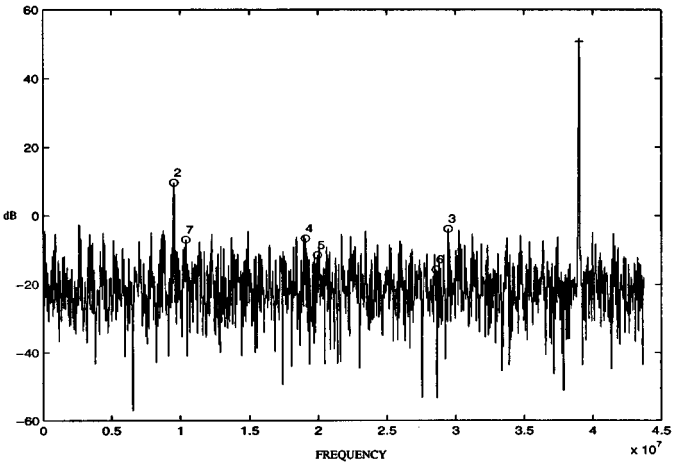

Fig. 19. Output spectrum (in dB) for the A/D converter, 6-bit mode. $F_{in} = 136$ MHz. $F_s = 700$ Msamples/s. Undersample ratio $= 8$.

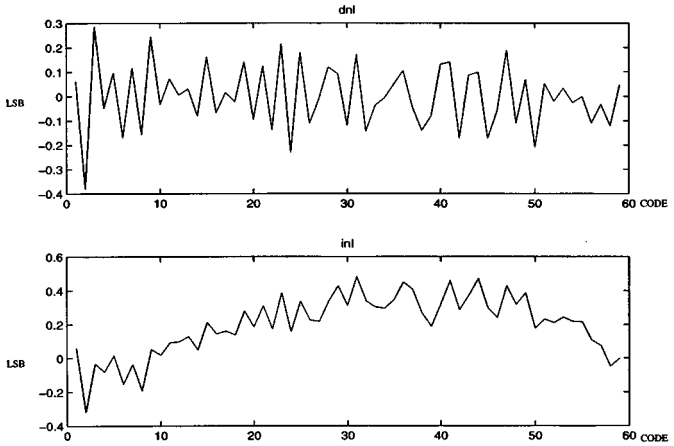

Fig. 20. DNL and INL (in LSB) for the A/D converter, 6-bit mode. $F_s = 700$ Msamples/s. x-axis shows the output code.

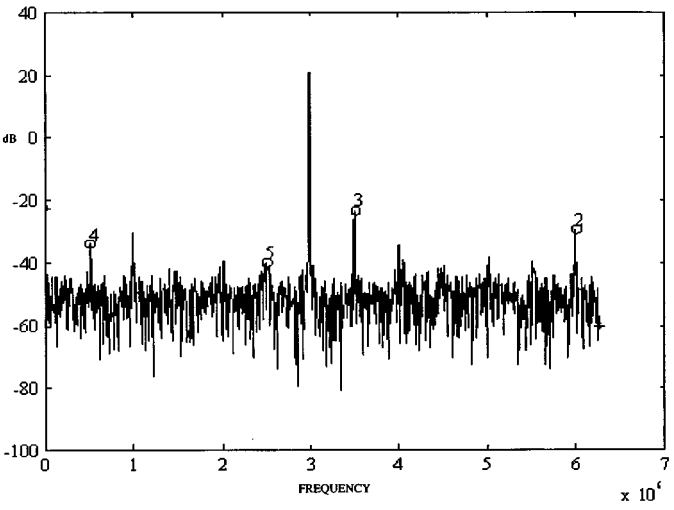

Fig. 21. Output spectrum (in dB) for the A/D converter, 7-bit mode. $F_{in} = 53$ MHz. $F_s = 200$ Msamples/s. Undersample ratio = 16.

In the 7-bit mode, at 200 MSamples/s, with 3.3 and 1.8-V supplies, the A/D converter consumes 143 mW of power. Fig. 21

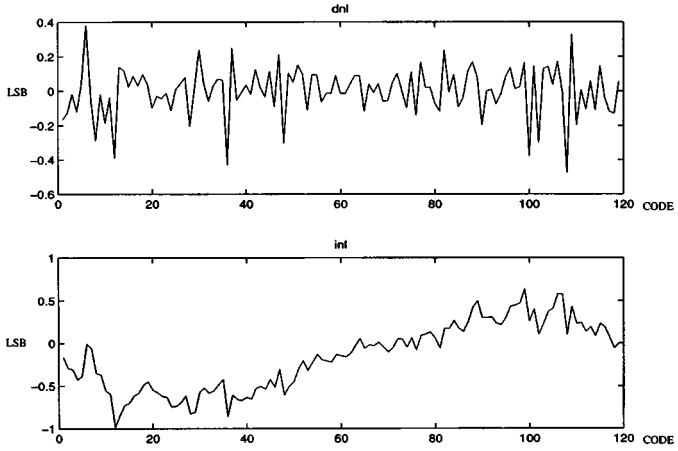

Fig. 22. DNL and INL (in LSB) for the A/D converter, 7-bit mode. $F_s = 200$ Msamples/s. x-axis shows the output code.

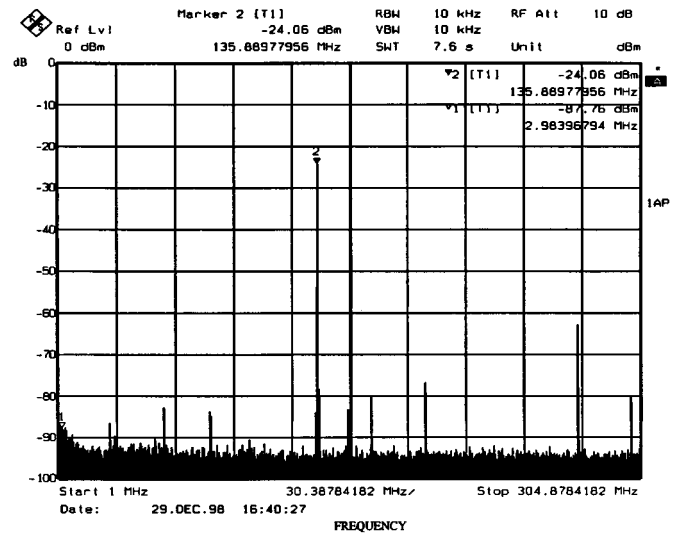

Fig. 23. Intermodulation distortion (in dB). $F_s = 600$ Msamples/s. $F_{in} = 136$ MHz. Intermodulation tone is at 164 MHz.

shows the output spectrum of the A/D converter output in the 7-bit mode; the SNDR is 40.66 dB for $F_{in} = 53$ MHz, $F_s = 200$ Msamples/s. Measured DNL and INL for the 7-bit mode are shown in Fig. 22.

To measure the intermodulation distortion due to the interleaving in the S/H, the S/H output was measured directly through a special test port that uses source follower buffers. The distortion due to interleaving is 56 dB below the fundamental, as shown in the measured spectrum in Fig. 23.

ACKNOWLEDGMENT

The authors would like to thank M. Chambers, A. Brewster, V. Pierotti, M. Spaeth, M. Peng, and B. Liebowitz for technical contributions, M. Barnett for assistance with the layout, and K. Kistner for assistance with the test board.

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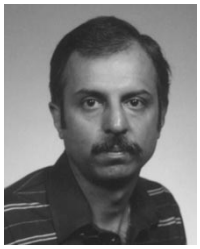

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