A BASEBAND PULSE SHAPING FILTER FOR GAUSSIAN MINIMUM SHIFT KEYING

N. Krishnapura[1], *S. Pavan*[2], *C. Mathiazhagan*[3], *B. Ramamurthi*[3]

[1] Department of Electrical Engineering, Columbia University, New York, NY 10027, USA
[2] Texas Instruments, Edison, NJ 08837, USA
[3] Department of Electrical Engineering, Indian Institute of Technology, Chennai, 600036, India
Email: nagi@elab.columbia.edu

ABSTRACT

Gaussian pulse shaping is used in digital communication systems like DECT, GSM, WLAN to minimize the out of band spectral energy. The baseband rectangular pulse stream is passed through a filter with a Gaussian impulse response before frequency modulating the carrier. Traditionally this is done by storing the values of the pulse shape in a ROM and converting it to an analog waveform with a DAC followed by a smoothing filter. This paper explores a fully analog implementation of an integrated Gaussian pulse shaper, which can result in a reduced power consumption and chip area.

1. INTRODUCTION

Gaussian pulse shaping of the baseband pulse stream is resorted to in digital communication systems like DECT and GSM in order to limit the spectral energy outside the transmission band. Gaussian Frequency Shift Keying (GFSK) [1] is a scheme where a Gaussian filtered pulse stream is used to frequency modulate the carrier. Conceptually, this is done by passing the baseband rectangular pulse stream (with values in $\{-1, 1\}$) through a filter with a Gaussian impulse response. The same can be thought of as adding or subtracting delayed versions of the unit pulse (one bit wide pulse of unit amplitude) response of the Gaussian filter depending on the sign of the input bit. The resulting "smoothed" stream is fed to a voltage controlled oscillator (VCO) as shown in (Fig. 1).

Traditionally, this pulse shaping is done digitally. In order to implement the system, the ideal unit pulse response which extends from $-\infty$ to $+\infty$ has to be truncated to some finite duration. The samples of the truncated step response are stored in a ROM. A DAC converts this digital data to a staircase waveform which is smoothed by a continuous time filter and fed to the VCO (Fig. 2).

In this paper, we describe a more direct realization of Fig. 1, using a continuous time filter whose impulse response is approximately Gaussian. We present the design of this filter and show that in many cases, the complexity of this filter is the same as that of the smoothing filter used in the digital approach. Effectively, the ROM and the DAC can be eliminated from Fig. 2, resulting in a reduction in the power consumption and chip area.

In the next section, we briefly discuss the GFSK system of Fig. 1. In section 3., we consider the design issues in a digital pulse shaping scheme. In section 4., we derive the continuous time Gaussian pulse shaping filter and present some simulation results demonstrating its suitability. Section 5. deals with the implementation of the pulse shaper in a 2 μm n–well CMOS process and the measurement results.

A quadrature modulation scheme to realize the same function as Fig. 1 can be derived. In this paper, we consider only the scheme shown in Fig. 1.

2. GAUSSIAN FREQUENCY SHIFT KEYING (GFSK)

The output of the system shown in Fig. 1 can be described by

$$y(t) = \cos(2\pi f_c t + 2\pi k_f \int_{-\infty}^{t} g(\tau)d\tau) \qquad (1)$$

where f_c is the unmodulated carrier frequency, k_f is the modulating index ($k_f = 0.25$ for Gaussian Minimum Shift Keying—GMSK[1]) and $g(\cdot)$ denotes the convolution of the rectangular bit stream $b(t)$ (with values in $\{-1, 1\}$) with the impulse response of the shaping filter (unity gain at dc) $h(t)$. The characterizing quantity of this system is the BT_b product, where B is the -3 dB bandwidth of the Gaussian filter and T_b is the bit period of the input stream. A smaller value of BT_b implies a longer response (relative to T_b) of the Gaussian filter to a unit pulse. Typical numbers for BT_b are in the range (0.3, 0.8). For $BT_b = 0.5$, the commonly used duration beyond which the unit pulse response is truncated is $3T_b$ ($\pm 1.5T_b$ from the peak).

3. DIGITAL PULSE SHAPING

The block diagram of a digital pulse shaping system is shown in Fig. 2. The input bit stream is fed into a shift register, whose length is equal to the number of bit durations over which the unit pulse response extends (for $BT_b = 0.5$, this is 3). The ROM contains the samples of the response of the Gaussian filter for every possible combination of the bit sequence in the shift register. If the Gaussian is sampled m times in every period and the pulse response extends over k bits, the ROM has $2^k \times m$ values stored in it.

The output of the ROM feeds a DAC. The staircase waveform at the output of the DAC is filtered using a continuous time filter before being fed to the VCO.

In commonly used communication systems, 6–8 bits are required in the DAC to keep the spurious emission due to the quantization error below the specified limit [2] [3] [4] [7]. For a given bit rate, a larger sampling rate relaxes the requirements on the smoothing filter, but this is difficult to achieve with high bit rates due to constraints on the power dissipation. For moderate sampling rates, the filter should have a large attenuation outside the band. In addition, it should have a *linear phase* in order not to distort the pulse shape. To satisfy both these criteria, a high order filter is necessary. To get a feel for the numbers, we note that in order to satisfy the DECT specifications, with $BT_b = 0.5$, 6 samples per bit duration and a 7–8

0-7803-4455-3/98/$10.00 © 1998 IEEE

bit DAC, a 7^{th} order bessel filter is required for smoothing [5]. With a low sampling rate, the filter also requires some automatic tuning scheme to set the cutoff frequency accurately.

4. ANALOG PULSE SHAPING

The hint towards obtaining a continuous time filter with a Gaussian impulse response comes from the "Central Limit Theorem" (CLT) in statistics. This states that the probability density function (pdf) of the sum of a large number of independent identically distributed random variables approaches a Gaussian. Since the pdf of the sum of random variables is obtained by convolving the individual pdfs, we infer that the cascade of a large number of identical filters (with positive impulse responses) has a Gaussian impulse response. This can be verified by cascading a large number of buffered first order RC sections.

As the name implies, CLT is a limiting result, and a realization with as small a number of impulse responses (a filter with as small an order as possible) is desirable in practice. To this end, we make the following generalizations.

- A cascade of large number of filters has a Gaussian impulse response.
- The impulse response of a filter with Gaussian magnitude response and linear phase is Gaussian.
- Bessel filter is optimized for linear phase.

With these facts in mind and with the aid of simulations, we conclude that a high order bessel filter results in a "sufficiently" Gaussian impulse response. Fig. 3 shows the step response of an 8^{th} order bessel filter and an ideal Gaussian filter for comparison.

By computer simulations, it is found that a 7^{th} order bessel filter satisfies the spectral specification of the DECT standards (suppression of energy outside the band). Note that this is the same order as that used for the smoothing filter in the digital pulse shaper (section 3.).

Fig. 4 shows the spectrum of the GMSK signal for a pseudo random input bit stream with an ideal Gaussian pulse shaper, for a digital pulse shaper with 10 samples per bit duration and different DAC resolutions and for a 7^{th} order bessel filter. It can be seen that the performance of the bessel filter is satisfactory.

5. 8^{th} ORDER BESSEL FILTER IN 2 μm CMOS TECHNOLOGY

The chip to be described is designed with the DECT specifications in mind, which uses a bit rate of 1.152 Mb/s and $BT_b = 0.5$. Therefore, an eighth order bessel filter with a bandwidth of 576 kHz is implemented. In order to set the bandwidth accurately, the filter is made tunable and an automatic frequency control loop is used.

The 8^{th} order filter is implemented as a cascade of biquads. Since the maximum Q factor is 1.23, Sallen–Key biquads can be used without having excessive sensitivity to component values. A single ended Sallen–Key biquad using a unity gain buffer, along with its transfer function, is shown in Fig. 5. To reduce the distortion due to the non linearity, two single ended filters are operated differentially. To make the filter tunable, the resistors are realized using nMOS transistors operating in the triode region. The common mode voltage is chosen to be 0.5 V in order to have sufficient room for the tuning voltage at the gate of the MOS resistors. The buffer used is a folded cascoded differential pair in unity gain feedback (Fig. 6). Two buffers are used for each differential biquad.

The control voltage for the MOS resistors is derived from the master–slave tuning scheme shown in Fig. 7 (see [6] for details of operation). The feedback loop forces the resonant frequency of the master filter (another tunable Sallen–Key biquad) to be equal to the reference frequency. By virtue of on chip component matching, the i^{th} biquad has a resonant frequency of (using the relations in Fig. 5)

$$\omega_{p,i} = 2\pi f_{ref}\sqrt{\frac{C_{1,ref}C_{2,ref}}{C_{1,i}C_{2,i}}} \qquad (2)$$

which, being a function of capacitor ratios, can be set accurately on a chip.

The reference frequency is chosen to be 2 MHz. The master filter is designed for $\omega_p = 2\pi \times 2$ MHz and $Q = 1$. The Q is kept low in order to avoid large voltage swings across the MOSFETs which would cause tuning errors due to nonlinearity and also to avoid large capacitor ratios (see the expressions in Fig. 5).

Cascoded differential pairs, operating in open loop, are used for the comparators in Fig. 7. The XOR gate drives a charge pump to realize the integrator in the loop. The details are not shown due to lack of space.

Fig. 8 shows the chip photograph. Fig. 9 shows the magnitude response for different reference frequencies. The step response is shown in Fig. 10. The impulse response is approximated by a response to a narrow pulse and is shown in Fig. 11. Slight asymmetry is apparent near the bottom of the output pulse, part of which is due to the finite width of the exciting pulse.

Table 1 summarizes the measured characteristics of the chip. The values given are the arithmetic mean and standard deviation for the 3 chips measured. The -3 dB frequency is tuned accurately. The maximum bandwidth is limited by the upper rail. The minimum bandwidth is zero, but for very small values of the control voltage, the MOS "resistors" in Fig. 5 operate with a small $|V_{GS} - V_T|$ and distort severely. The lower limit is assumed to be the point where a $1V_{pp}$ input at 50 kHz has a THD of -40 dB. The distortion measurements are made with a single input tone at 50 kHz (whose harmonics are inside the passband) and also at 576kHz. The distortion in a Sallen–Key low pass filter increases with frequency due to increased drop across the MOS resistors. Since the bit rate is 1.152 MHz, the "fastest" input is a 576 kHz square wave. The performance with a 576 kHz sinusoidal input is given as a measure of the worst case. In practice, the inputs have their energy concentrated at frequencies lower than 576 kHz.

6. CONCLUSION

This paper describes the design of an analog Gaussian pulse shaping chip for use in digital communication systems. Simulation results demonstrating the feasibility of this scheme are shown. It is shown that for large bit rates, the pulse shaping can be done with circuitry equivalent in complexity to the smoothing filter in the digital shaping method, when a VCO is used for GFSK modulation. A pulse shaping filter with a -3dB bandwidth of 576 kHz for DECT cordless telephone applications is fabricated in 2 μm n–well Orbit CMOS technology. Measurement results are given.

Table 1. Summary of the measured characteristics

Technology	2 μm n-well CMOS
Supply voltage	3.3 V
Chip area	2.3 mm^2
Capacitance	63.8 pF (slave)
	9.9 pF (master)
Reference (nom.)	2 MHz, sinusoidal
Power consumption	9.2 ± 0.24 mW
dc gain	-0.27 ± 0.05 dB
dc offset	15 ± 9.8 mV
f_{-3dB}, nom	577.7 ± 9.7 kHz
f_{-3dB}, max	692.3 ± 21.5 kHz
f_{-3dB}, min	424 ± 8.2 kHz
output noise (upto 5 MHz)	409 ± 5.7 μV
Ref. feedthrough	-70.6 ± 0.32 dB
50 kHz test tone:	
$V_{i\,pp,max}$ $(THD \leq 40\,dB)$	1.63 ± 0.06 V
Dyn. range $(THD \leq 40\,dB)$	63.7 ± 0.57 dB
$S/(N+D)$ when $THD = N$	52.8 ± 0.38 dB
576 kHz test tone:	
$V_{i\,pp,max}$ $(THD \leq 40\,dB)$	557 ± 40 mV
Dyn. range $(THD \leq 40\,dB)$	53.6 ± 0.73 dB
$S/(N+D)$ when $THD = N$	46.1 ± 0.48 dB

References

[1] K. Murota & K. Hirade, "GMSK Modulation for Digital Mobile Radio Telephony", *IEEE Transactions on Communications*, vol. 29, pp. 1044–50, Jul. 1981.

[2] Alfredo Linz & Alan Hendrickson, "Efficient Implementation of an I–Q GMSK Modulator", *IEEE TCAS–II*, vol.43, no.1, pp. 14–23 , Jan. 1996.

[3] B. Baggini et al., "Integrated Digital Modulator and Analog Front-End for GSM Digital Cellular Mobile Radio System", *Proc. IEEE 1991 CICC* vol. 31, pp. 7.6.1–4, Mar. 1991.

[4] D. Sallaerts et al., "Efficient Implementation of an I–Q GMSK Modulator", *Digest 1990 IEEE ISSCC*, pp. 336, 345

[5] F. Yang & C. Enz, "A Low Distortion Seventh Order Bessel Filter Operating at 2.5 Volts Supply", *Proc. IEEE 1995 CICC*, pp. 551–554.

[6] Y. P. Tsividis and J. O. Voorman (eds.), *Integrated Continuous Time Filters*, IEEE Press 1992.

[7] *Specification for the DECT ARi^{1TM} Interface to the Radio Frequency Front End*, National Semiconductor App. Note 908, Sep. 1993.

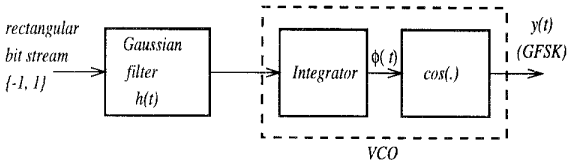

Figure 1. GFSK signal Generation

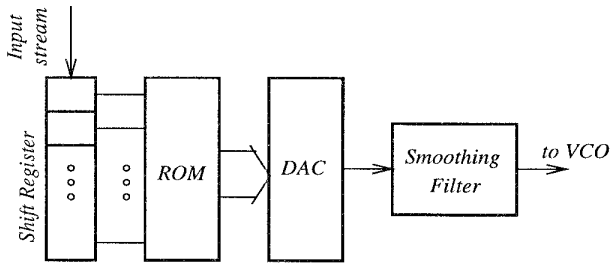

Figure 2. Digital Gaussian Pulse Shaper

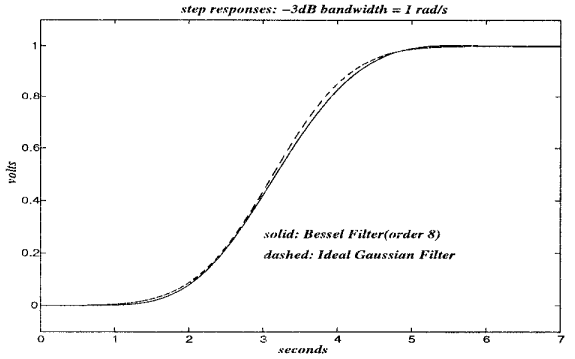

Figure 3. Step Responses

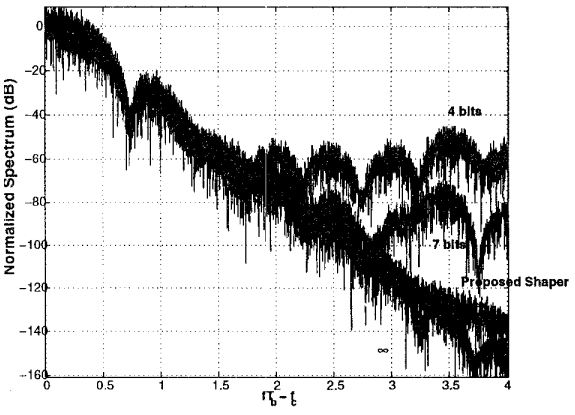

Figure 4. GMSK Spectrum with Different Pulse Shapers

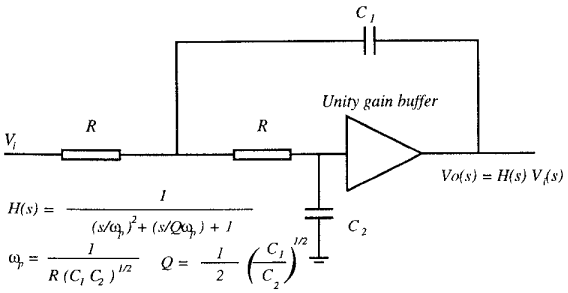

Figure 5. 2^{nd} order Sallen–Key Filter

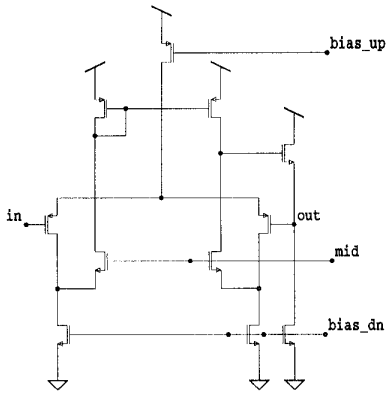

Figure 6. Unity Gain Buffer

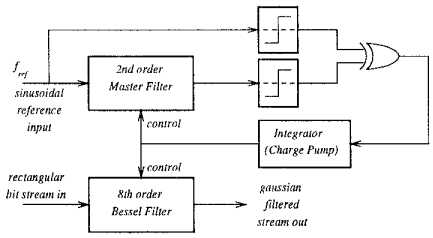

Figure 7. Frequency Tuning Loop

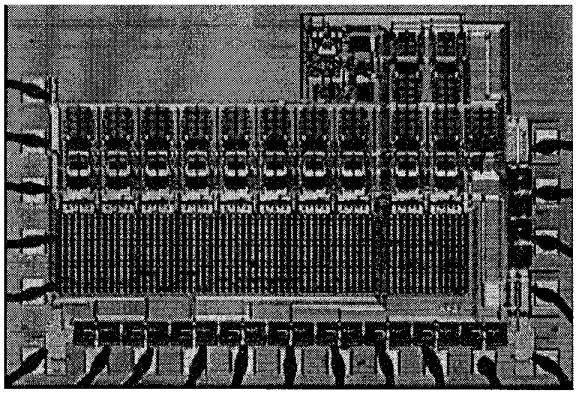

Figure 8. Chip Photograph

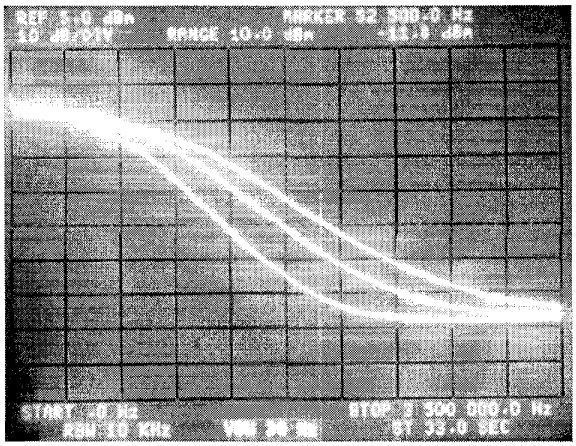

Figure 9. Frequency Response: f_{ref} = 1.4, 1.8, 2.2 MHz

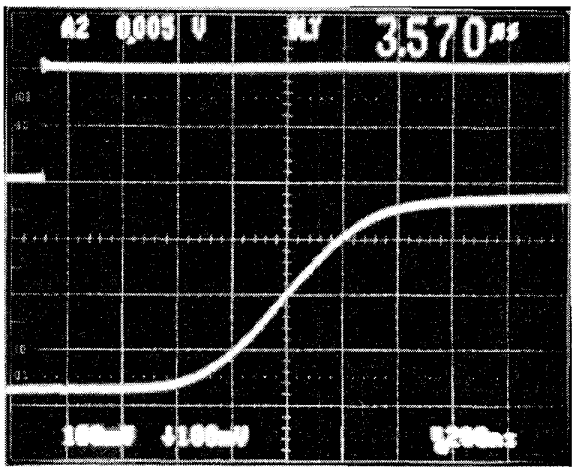

Figure 10. Fabricated Filter Step Response

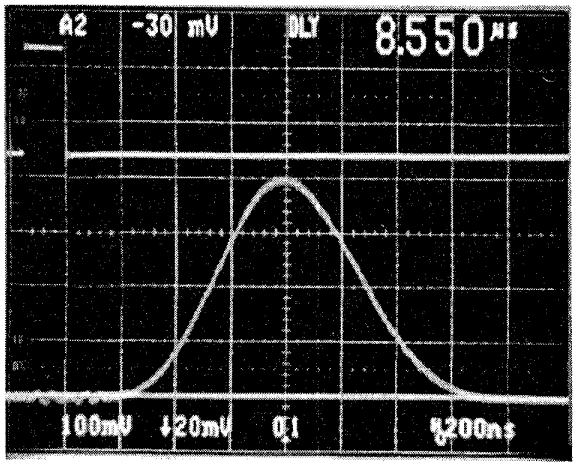

Figure 11. Response to a Narrow Pulse