MODELING OF ACCUMULATION MOS CAPACITORS FOR ANALOG DESIGN IN DIGITAL VLSI PROCESSES

Shanthi Pavan†, Yannis Tsividis‡
Krishnaswamy Nagaraj†

†Texas Instruments
Warren, New Jersey NJ 07059

‡ Department of Electrical Engineering
Columbia University, New York NY 10027

OUTLINE

- Introduction
- The two terminal MOS structure in accumulation
- Model implementation
- The polysilicon gate depletion effect
- Measurement results and discussion
- Conclusions

INTRODUCTION

- High density poly-poly capacitors are not available in low cost digital CMOS technologies.

- Metal-metal structures have very low specific capacitance.

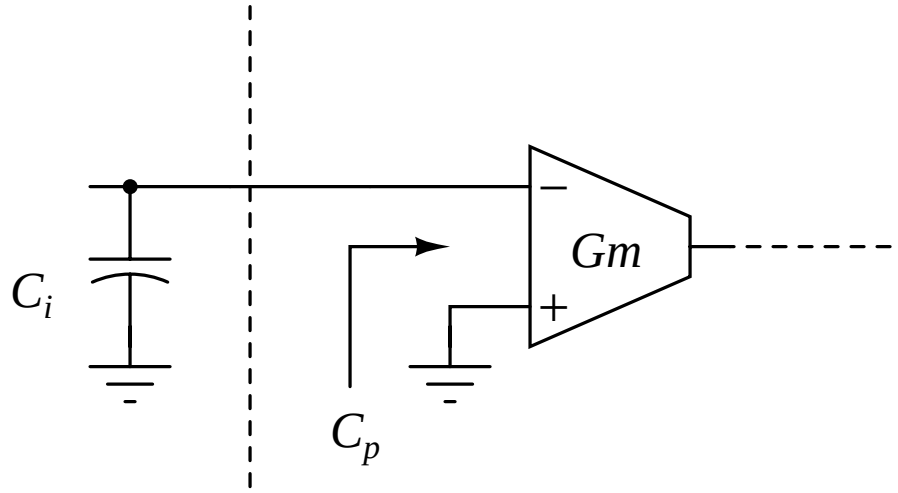
- Alternative is to use the "flat" parts of the C-V curve of a two terminal MOS capacitor.

For example, in a $0.25\,\mu$m CMOS process

$$C'_{ox} \approx 7.5\,\text{fF}/\mu\text{m}^2$$

Metal-metal edge capacitors have densities of about $0.5\,\text{fF}/\mu\text{m}^2$ (4 metal layers).

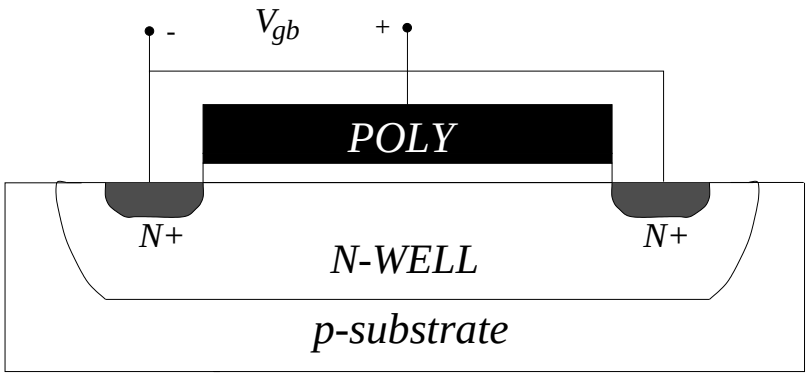
OTHER BENEFITS OF MOS CAPACITORS



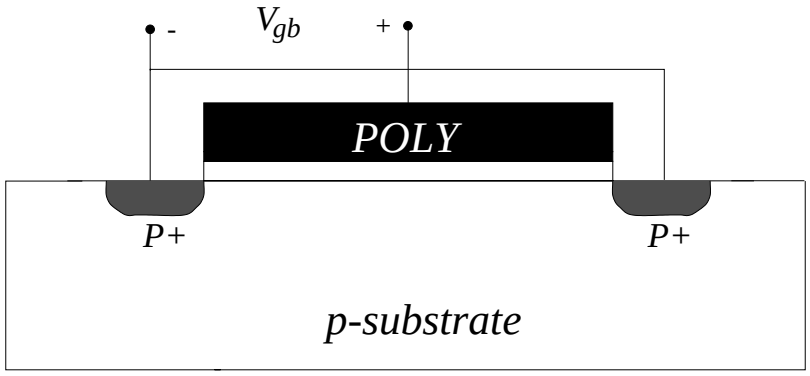
Example :Parasitics match integrating capacitors in filters

More accurate capacitor ratios because the integrating capacitors and parasitics track over process and temperature (useful in continuous-time filters)

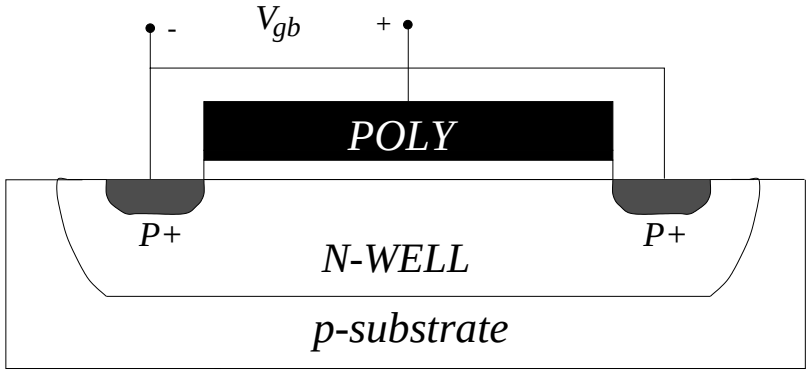
MOS CAPACITOR STRUCTURES IN *n*-WELL CMOS PROCESSES



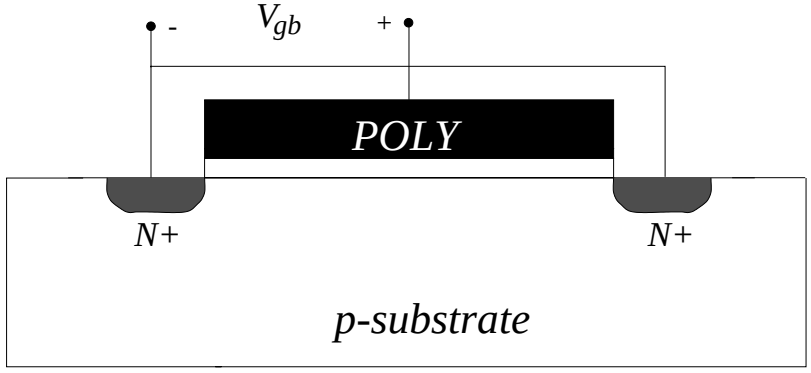
(a) Accumulation



(a) Accumulation



(b) Inversion



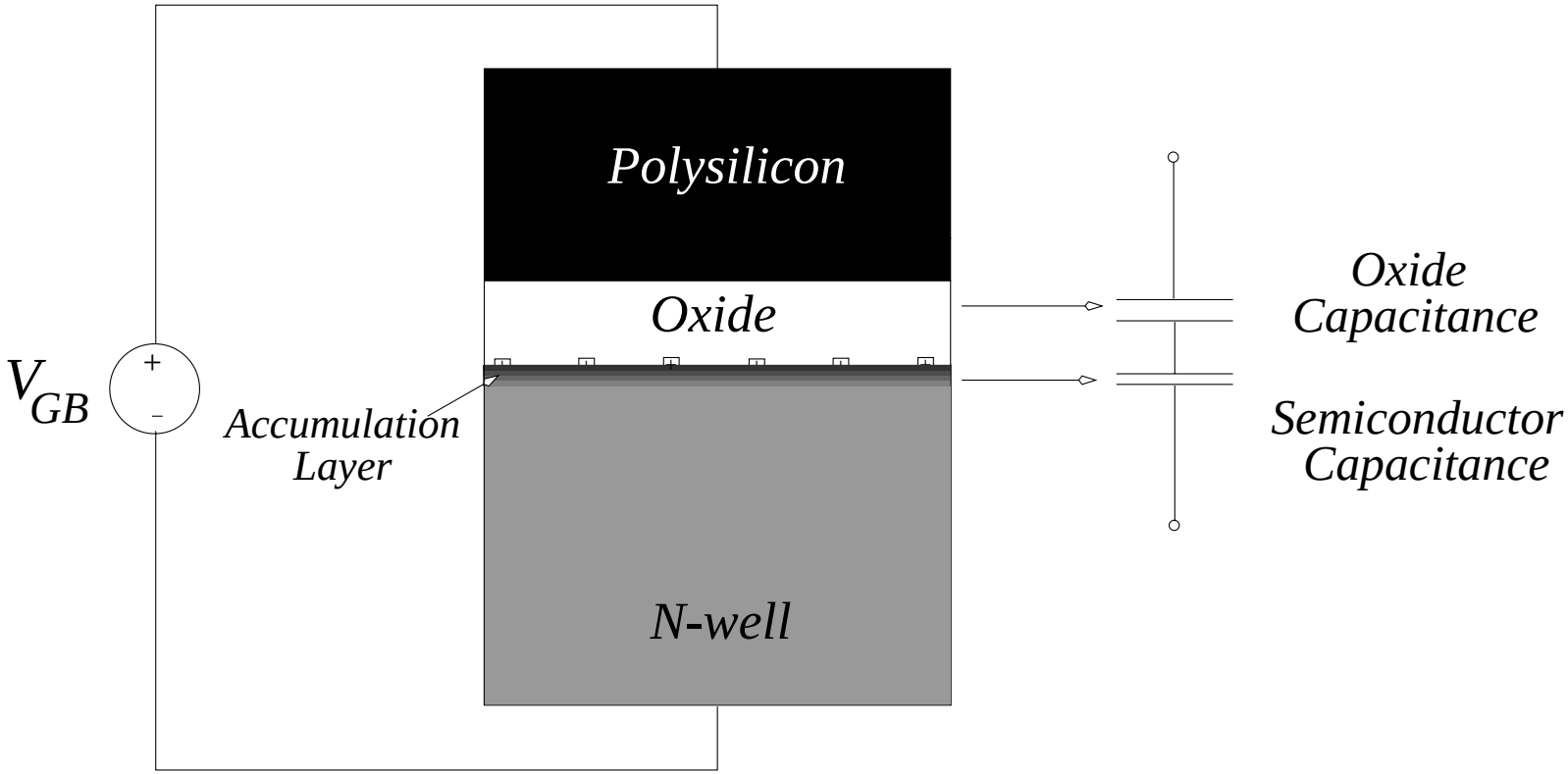
(b) Inversion

MOTIVATION

- It has been shown (by Behr et. al) that operation in accumulation is preferable to operation in inversion.
- For analog design, derivatives of the C-V curve must be accurately modeled.
- Existing SPICE models totally inadequate in accumulation.

THE POLY-n-WELL MOS CAPACITOR

In accumulation, holes in the n-well can be neglected



CALCULATING C'_{gb}

- For a given V_{GB}, solve for ψ_s the equation

$$V_{GB} = V_{FB} + \psi_s + \gamma\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t} \tag{1}$$

- Use the ψ_s obtained above in the following to get C'_c

$$C'_c = \frac{\gamma C'_{ox}(\exp(\frac{\psi_s}{\phi_t}) - 1)}{2\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t}} \tag{2}$$

- Use C'_c in the following to get C'_{gb}

$$C'_{gb} = \frac{C'_{ox}C'_c}{C'_{ox} + C'_c} \tag{3}$$

An explicit model would be more convenient.

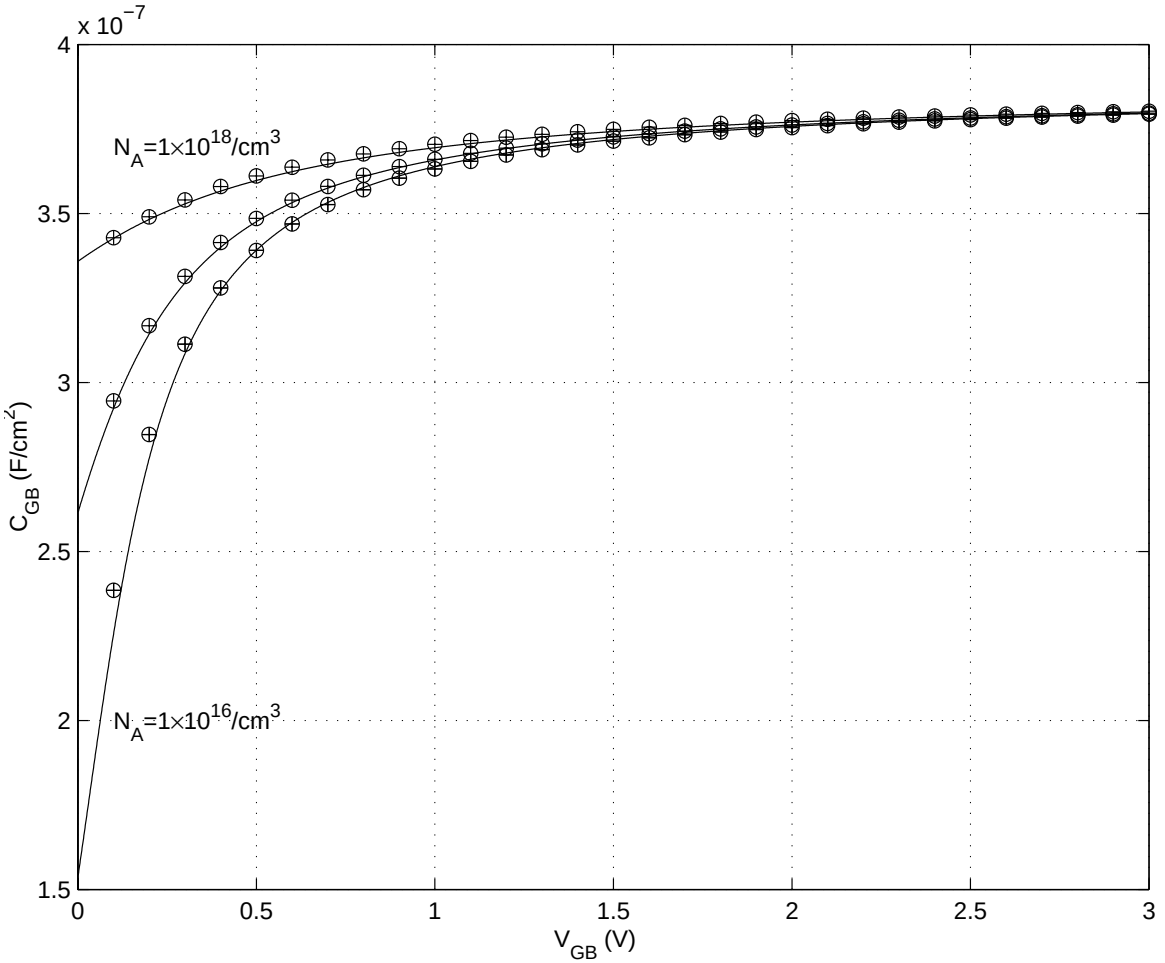
AN EXPLICIT EXPRESSION FOR THE SURFACE POTENTIAL

It can be shown that an approximate explicit expression for the surface potential is :

$$\psi_s = 2\phi_t \left[\frac{V_{GB} - V_{FB} + 3\phi_t}{V_{GB} - V_{FB} + 6\phi_t}\right] \log\left(1 + \frac{V_{GB} - V_{FB}}{\gamma\sqrt{\phi_t}}\right) \qquad (4)$$

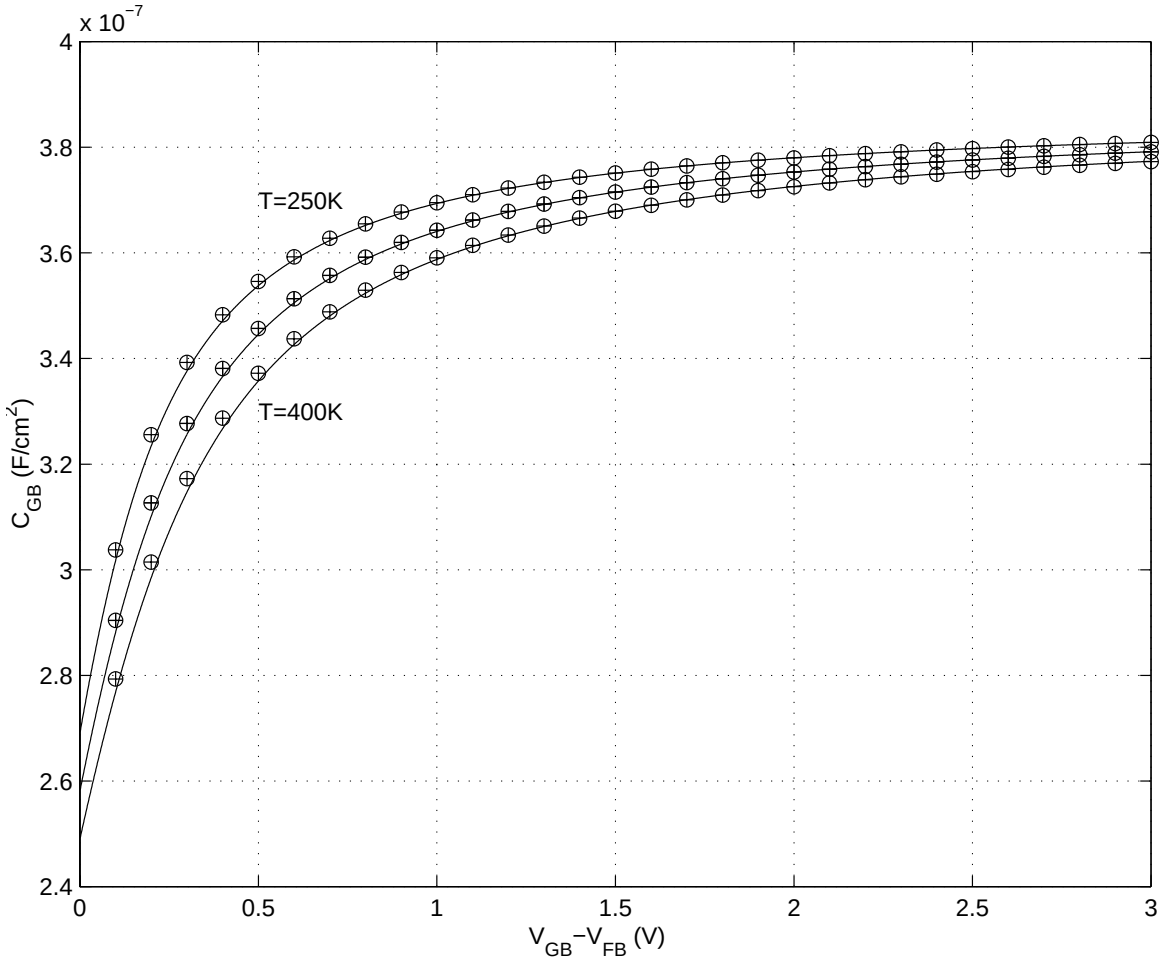
Using this, the capacitance of the structure can be calculated.

MODEL VALIDATION



Comparison of numerical simulation and proposed models for changes in substrate doping concentrations (– numerical, $\oplus$ proposed).
$C'_{ox} = 3.84\,\text{fF}/\mu\text{m}^2$, $V_{FB} = 0$, T=300 K.

MODEL VALIDATION



Variation of Capacitance with Temperature(– numerical, $\oplus$ proposed).

$C'_{ox} = 3.84\,\mathrm{fF}/\mu\mathrm{m}^2$, $V_{FB} = 0$, $N_D = 10^{17}\,\mathrm{cm}^{-3}$.

MODEL IMPLEMENTATION IN SPICE

.TRAN analysis $\Rightarrow Q'_G$ (Gate charge per unit area) is needed.
There are 2 ways of doing this.

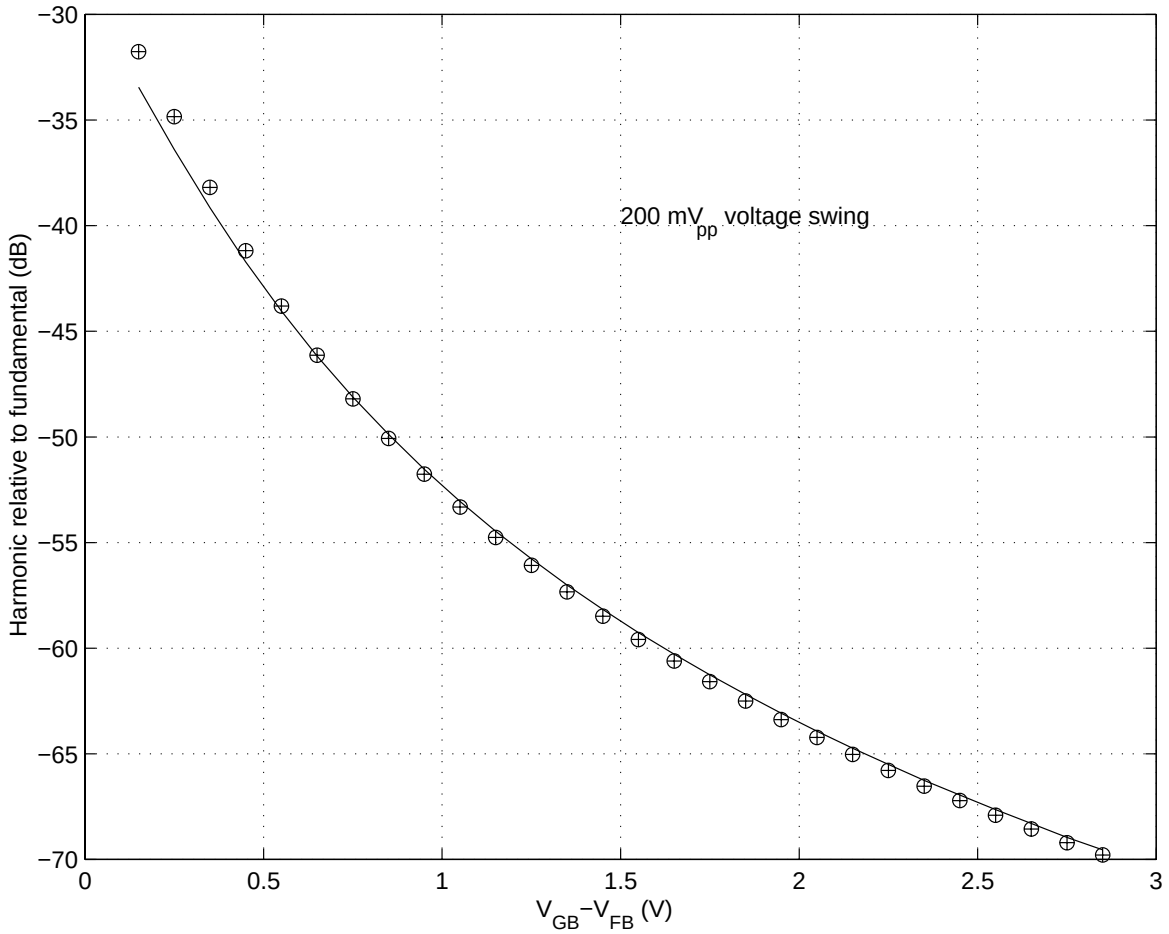
$$Q'_G = -Q'_c - Q'_o = \sqrt{2q\epsilon_s N_D}\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t} - Q'_o \qquad (5)$$

$\Rightarrow$ Very sensitive to the value of ψ_s ! (BAD)

$$Q'_G = C'_{ox}\psi_{ox} = C'_{ox}(V_{GB} - \psi_s - \phi_{MS}) \qquad (6)$$

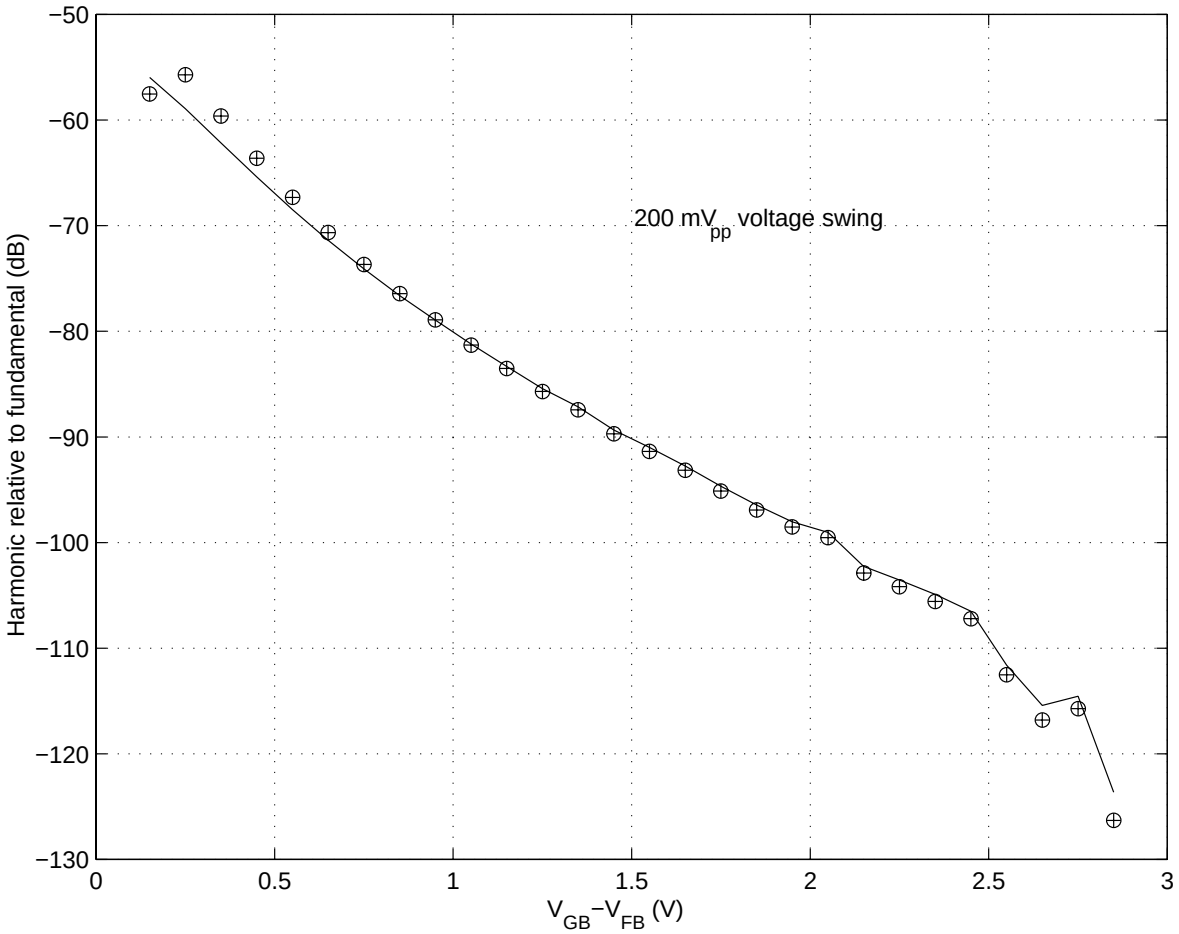
$\Rightarrow$ Less sensitive to the value of ψ_s. (GOOD)

DISTORTION COMPARISON WITH A FINELY SPACED PWL DATA FROM DEVICE SIMULATION



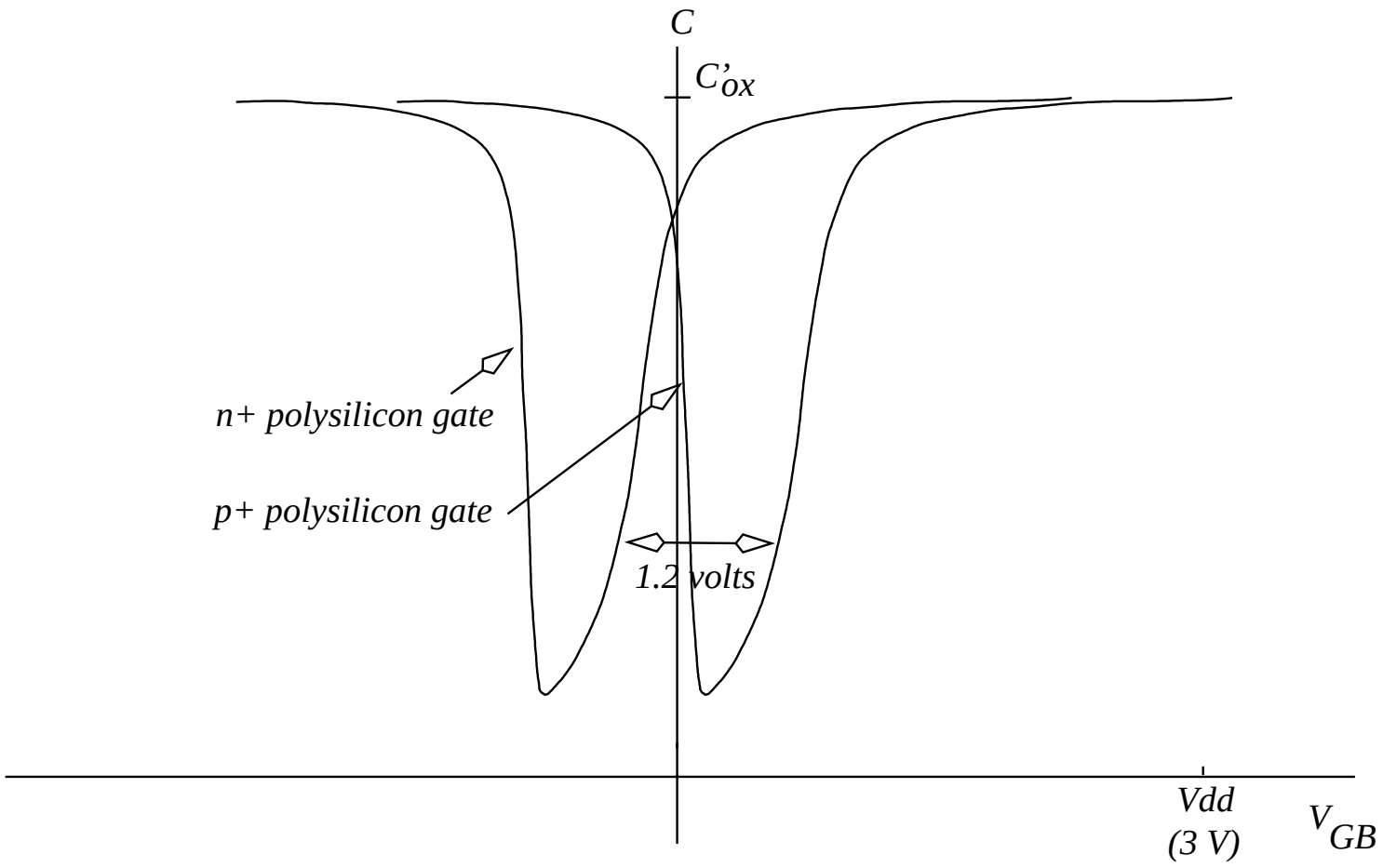
Second harmonic relative to fundamental(– PWL, $\oplus$ proposed)

DISTORTION COMPARISON WITH A FINELY SPACED PWL DATA FROM DEVICE SIMULATION



Third harmonic relative to fundamental(– PWL, $\oplus$ proposed)

CIRCUIT CONSIDERATIONS AND CHOICE OF POLYSILICON TYPE

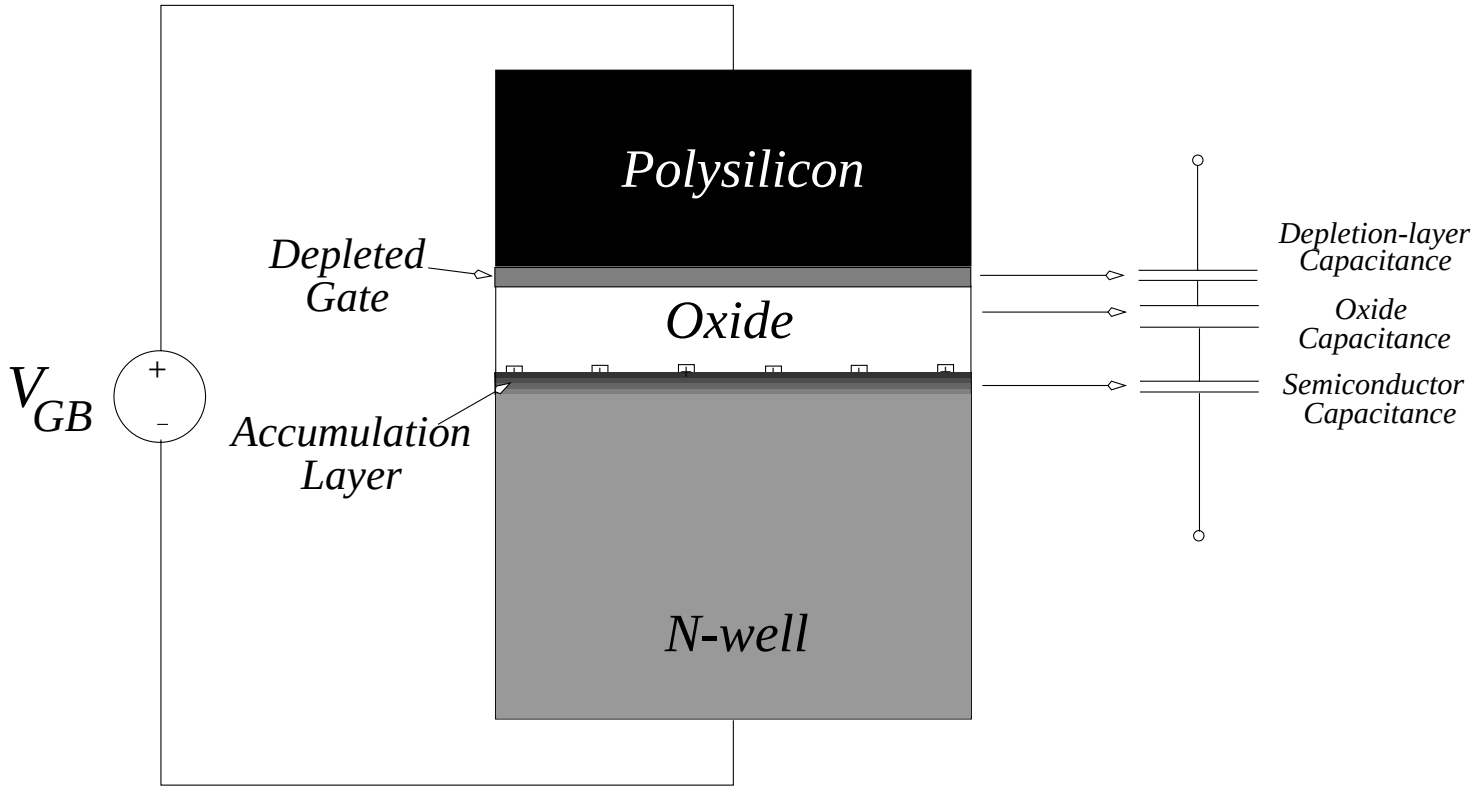


For circuit work, we need the structure to be in strong accumulation for as low a bias voltage as possible $\Rightarrow$ V_{FB} should be as negative as possible $\Rightarrow$ Use n-type polysilicon.

THE POLYSILICON GATE DEPLETION EFFECT

- It is not possible to dope the gate infinitely high with donors.

- Finite doping levels in the gate cause a thin gate depletion layer.



THE POLYSILICON GATE DEPLETION EFFECT

- The capacitance of this layer appears in series with C'_{ox} and C'_c.

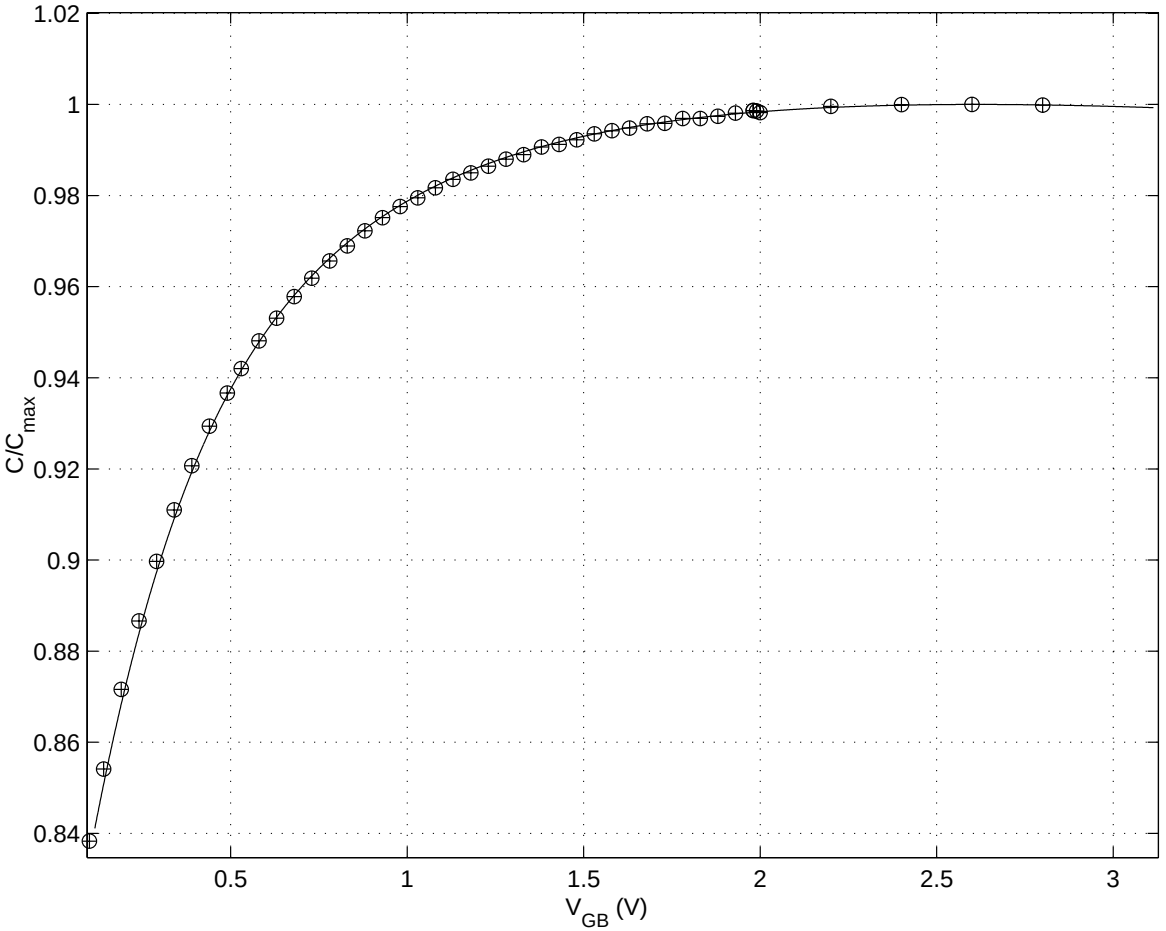
$$\frac{1}{C'_{gb}} = \frac{1}{C'_{ox}} + \frac{1}{C'_c} + \frac{1}{C'_{dep}} \tag{7}$$

$$C'_{dep} \approx \frac{\gamma_p^2 C'_{ox}}{2(V_{GB} - \phi_{MS} - \psi_s)} \tag{8}$$

where

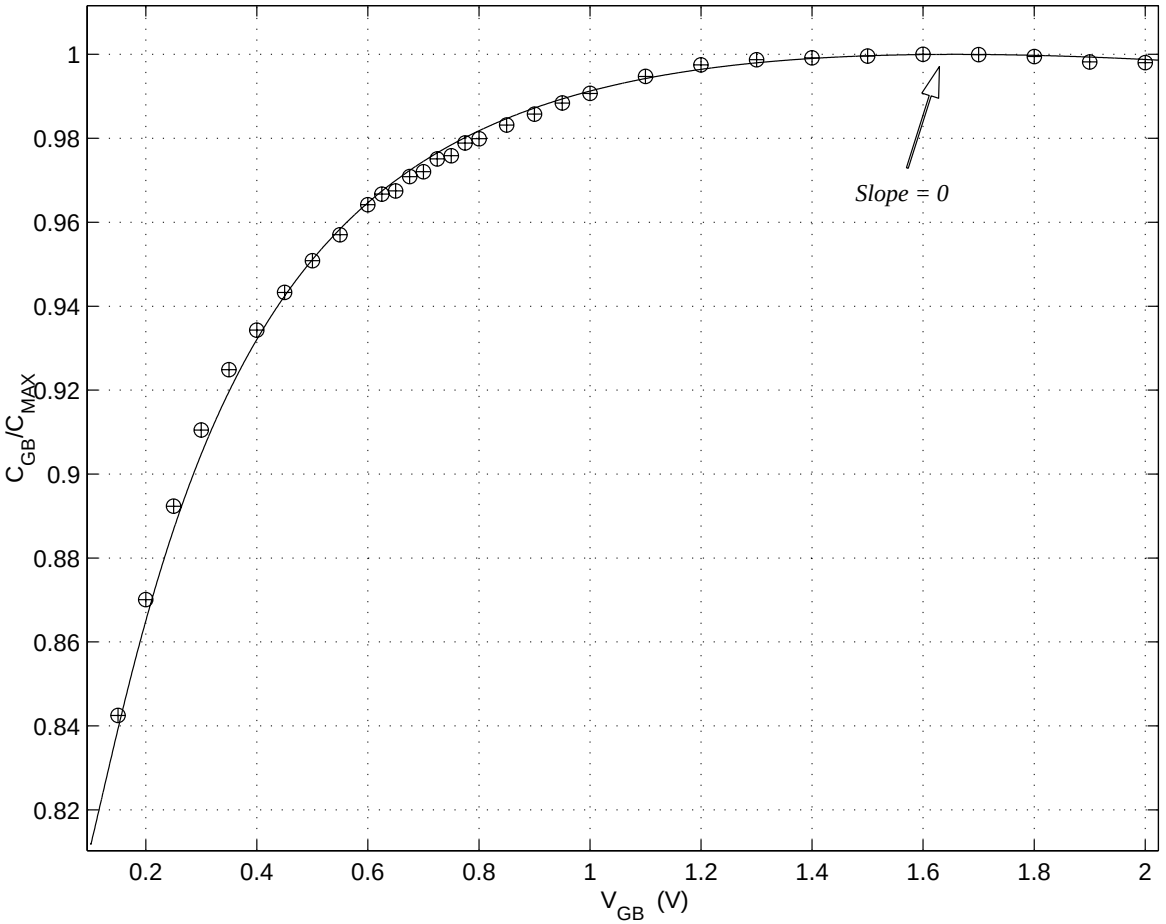
$$\gamma_p = \frac{\sqrt{2q\epsilon_s N_{POLY}}}{C'_{ox}} \tag{9}$$

COMPARISON WITH MEASURED DATA



Comparison for a 84 Å gate oxide capacitor (–model, $\oplus$ data).

COMPARISON WITH MEASURED DATA



Comparison for a 45 Å gate oxide capacitor (–model, $\oplus$ data).

CONCLUSIONS

- An explicit model has been proposed for a MOS capacitor in accumulation.
- The polysilicon gate depletion effect has been incorporated into the model.
- The model accurately predicts distortion, which is useful in analog design.
- The model has been implemented in SPICE.