MODELING OF ACCUMULATION MOS CAPACITORS FOR ANALOG DESIGN IN DIGITAL VLSI PROCESSES

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ABSTRACT

In this paper, we present an explicit model for the MOS capacitor in accumulation and compare it with device simulation and measurement results. The model is physics based and tracks substrate doping concentration and temperature, and incorporates the polysilicon gate depletion effect. Harmonic distortion generated when the proposed model is used in circuit simulation agrees with that obtained by using a very closely spaced piecewise linear model generated by device simulation.

1. INTRODUCTION

There has been a growing interest in implementing mixed analog–digital systems on a single chip. For economical reasons, the preferred technology is CMOS. In low-cost digital CMOS processes, high density poly-poly capacitors are not available. Metal-metal capacitors can be used, but their specific capacitance is very low. The focus of this work is the use of MOS capacitors *in place of* metal-metal capacitors. This means that the regions of interest are the "flat" parts of the C–V characteristic. A two terminal MOS structure can be operated in accumulation or inversion. It can be shown that for typical process parameters, and a given gate-body bias, accumulation capacitors tend to be more linear. For this the reader is referred to an excellent paper [1]. Hence, we do not consider inversion capacitors. Moreover, existing SPICE MOS transistor models are not accurate in accumulation since it is typically not important for transistor operation. The above two factors are the motivation behind this work.

In this paper, we present an explicit physics-based simulation model for the two-terminal MOS capacitor in accumulation. In Section 2, we derive the model from first principles and compare it with results obtained by numerical solution of the device equations. Model implementation issues are considered in Section 3. In deep submicron CMOS technologies, it is not possible to dope the gate with arbitrarily high concentrations of acceptors/donors. Then the assumption that the potential throughout the gate is constant is not valid anymore. Finite gate doping causes what is known as the "polysilicon gate depletion effect." This phenomenon is analyzed and incorporated into our model in Section 4. Section 5 compares the complete model derived in Section 4 to capacitor measurements in some typical fine line CMOS processes. Section 6 contains the conclusions of this work.

2. THE TWO TERMINAL MOS STRUCTURE

Consider the two–terminal poly–n-well MOS structure shown in Figure 1. For a given bias voltage V_{GB} applied across the device, we present relations for charge, capacitance and surface potential. Derivations are not shown here for lack of space, the reader is referred to [2]. ψ_{ox} is the potential drop across the oxide. ψ_s is the surface potential. ϕ_{MS} is the potential corresponding to the work function difference of the bulk and the gate materials. Q'_G

and Q'_c denote the charge per unit area on the gate and in the semiconductor respectively. Q'_o is the effective interface charge per unit area of the oxide. ϵ_s, N_D and ϕ_t stand for the permittivity of silicon, donor density in the n-well and the thermal voltage respectively. C'_{ox} is the capacitance of the oxide per unit area and ϕ_F is the Fermi potential of the n-well. Using Kirchhoff's voltage law and charge conservation along with Poisson's equation in the y-direction, it can be shown that in accumulation, after neglecting the presence of holes in the n-well [2],

$$Q'_c = -\sqrt{2q\epsilon_s N_D}\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t} \qquad (1)$$

$$V_{GB} = V_{FB} + \psi_s + \gamma\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t} \qquad (2)$$

$$Q'_G + Q'_c + Q'_o = 0 \qquad (3)$$

where

$$\gamma = \frac{\sqrt{2q\epsilon_s N_D}}{C'_{ox}} \qquad (4)$$

$$V_{FB} = \phi_{MS} - \frac{Q'_o}{C'_{ox}} \qquad (5)$$

For a given bias V_{GB}, we can solve (2) numerically for ψ_s and calculate Q'_c using (1). However, if an explicit expression for the surface potential can be obtained, calculations become much more straightforward. It can be found that, for typical values of γ and temperature, such an explicit expression is (see Appendix A),

$$\psi_s = 2\phi_t \left[\frac{V_{GB} - V_{FB} + k_1\phi_t}{V_{GB} - V_{FB} + k_2\phi_t}\right] \log\left(1 + \frac{V_{GB} - V_{FB}}{\gamma\sqrt{\phi_t}}\right) \qquad (6)$$

where $k_1 = 3$ and $k_2 = 6$ provide a good fit to a numerical solution of (2), for a wide range of process parameters. The capacitance of the two-terminal structure per unit area C'_{gb} is obtained from

$$\frac{1}{C'_{gb}} = \frac{1}{C'_{ox}} + \frac{1}{C'_c} \qquad (7)$$

where $C'_c = -\frac{dQ'_c}{d\psi_s}$ is the capacitance of the accumulation layer per unit area. Differentiating (1),

$$C'_c = \gamma C'_{ox} \frac{\exp(\frac{\psi_s}{\phi_t}) - 1}{2\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t}} \qquad (8)$$

Figure 2 compares the capacitance obtained by numerical methods with the explicit model proposed in this paper. C'_{ox} was kept constant and the N_D values used were 10^{16}cm^{-3}, 10^{17}cm^{-3} and 10^{18}cm^{-3}. Note that this corresponds to the variation of γ by a factor of ten.

3. MODEL IMPLEMENTATION

In this section we examine issues that arise in implementing the model in a general purpose circuit simulator. In this work, the model was implemented in TISPICE, an in-house circuit simulation program at Texas Instruments. The model is implemented as a user defined utility, coded as a 'C' routine. C'_{gb} is calculated using (7) for use in AC simulations. For transient simulations, Q'_G is needed. One needs to be careful with the way in which it is obtained. One could use (3) and (1) to obtain

$$Q'_G = -Q'_c - Q'_o = \sqrt{2q\epsilon_s N_D}\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t} - Q'_o$$

(9)

Alternatively

$$Q'_G = C'_{ox}\psi_{ox} = C'_{ox}(V_{GB} - \psi_s - \phi_{MS})$$ (10)

The two approaches would yield identical results *if ψ_s was known exactly*. However, our expression (6) for ψ_s is approximate. When the applied gate bias is very large, even a small error in determining the surface potential would lead to a large error in computing charge from (9). On the other hand, (10) has no such problem. Hence, this expression should be used to calculate capacitor charge.

The performance of the implemented model was compared with a very finely spaced (voltage steps of 1 mV) piecewise linear capacitor model generated from device simulation. A MOS capacitor was driven with a sinusoidal voltage source and the distortion in the capacitor current was used as a metric for comparison of the two models. Distortion depends on *derivatives* of the C–V characteristic, and is hence a very sensitive indicator of modeling accuracy. Since third harmonic distortion is very small at high bias voltages and/or low signal levels, simulations were run at very tight tolerances, and using a very small timestep compared to the period of the voltage source. The dynamic range of the simulations is about 100 dB. Figure 3 and 4 compare the levels of second and third harmonic currents.

3.1. Circuit considerations and choice of polysilicon type

Until now, the results we derived for Q'_G, Q'_c and ψ_s were independent of the type of polysilicon used as the gate material. We now examine the two choices for the the type of polysilicon (n or p) from a circuit design viewpoint. As mentioned in the introduction to this paper, we are interested in using MOS accumulation capacitors in place of metal-metal capacitors. We would like to be operating in deep accumulation even for a very small V_{GB}. Hence, the flatband voltage (V_{FB}) should be as negative as possible. In modern CMOS technologies C'_{ox} is very large, and the term $\frac{Q'_o}{C'_{ox}}$ in (5) is typically about 100 mV. If the gate is degenerately doped (either $n+$ or $p+$), ϕ_{MS} is given by

$$\phi_{MS} = \begin{cases} -\phi_F - 0.56V \ , & n+ \text{ poly} \\ -\phi_F + 0.56V \ ; & p+ \text{ poly} \end{cases}$$ (11)

From the above equation, $n+$ polysilicon is the one of choice. We will henceforth assume that this is the case.

4. THE POLYSILICON GATE DEPLETION EFFECT

The analysis presented in the preceding sections assumes that the "top plate" of the MOS capacitor is infinitely highly doped. In practice, the finite doping density of the $n+$ polysilicon causes a depletion layer in the gate, whose thickness depends on the amount of negative charge in

the n-well. In the literature[3][4], the effects of gate depletion are analyzed when the MOS structure is in inversion. Accumulation is not considered as this region is not important for transistor operation.

We redraw the cross section of the MOS capacitor in Figure 5, now with a depletion layer in the gate. Assume that the gate is uniformly doped n type with a donor concentration of N_{POLY}. Let ψ_{dep} denote the potential drop across the gate depletion layer. Let a voltage V_{GB} we applied to the structure as shown. The potential balance equation can be written as

$$V_{GB} = \phi_{MS} + \psi_{dep} + \psi_{ox} + \psi_s$$ (12)

Charge balance as given by (3) still holds. Using this along with $\psi_{ox} = Q'_G/C'_{ox}$ in (12), we get

$$V_{GB} = \phi_{MS} + \psi_{dep} - \frac{Q'_c + Q'_o}{C'_{ox}} + \psi_s$$ (13)

Using (5), the above equation can be rewritten as

$$V_{GB} = V_{FB} + \psi_{dep} + \psi_s - \frac{Q'_c}{C'_{ox}}$$ (14)

Q'_c is only a function of ψ_s and is given by (1). Using (1) with (14)

$$V_{GB} = V_{FB} + \psi_s + \psi_{dep} + \gamma\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t}$$ (15)

From basic electrostatics,

$$Q'_G = \sqrt{2q\epsilon_s N_{POLY}}\sqrt{\psi_{dep}}$$ (16)

Using $Q'_G = C'_{ox}\psi_{ox}$ alongwith (12) we have

$$Q'_G = C'_{ox}\psi_{ox} = C'_{ox}(V_{GB} - \phi_{MS} - \psi_s - \psi_{dep})$$ (17)

Hence,

$$\sqrt{2q\epsilon_s N_{POLY}}\sqrt{\psi_{dep}} = C'_{ox}(V_{GB} - \phi_{MS} - \psi_s - \psi_{dep})$$ (18)

Defining $\gamma_p = \frac{\sqrt{2q\epsilon_s N_{POLY}}}{C'_{ox}}$ enables us to rewrite (18) as

$$\psi_{dep} + \gamma_p\sqrt{\psi_{dep}} - (V_{GB} - \phi_{MS} - \psi_s) = 0$$ (19)

Assuming ψ_s is known, the above equation can be solved to give

$$\psi_{dep} = \left(-\frac{\gamma_p}{2} + \frac{\gamma_p}{2}\sqrt{1 + \frac{4}{\gamma_p^2}(V_{GB} - \phi_{MS} - \psi_s)}\right)^2$$ (20)

To get simpler analytic expressions, (20) can be further simplified by noting that for practical values of process parameters and reasonable bias voltages, $\frac{\gamma_p^2}{4} >> V_{GB}$. Hence, (20) can be simplifed to give

$$\psi_{dep} = \frac{1}{\gamma_p^2}(V_{GB} - \phi_{MS} - \psi_s)^2$$ (21)

In order to compute ψ_s, (20) (or the simplified form (21)) should be used for ψ_{dep} in (15). The resulting equation is implicit and even more complicated that (2). Since $\frac{\gamma_p^2}{4} >> V_{GB}$, ψ_{dep} is a very small fraction of V_{GB}. Hence,

we can neglect ψ_{dep} on the right hand side of (15), which can now be written as

$$V_{GB} = V_{FB} + \psi_s + \gamma\sqrt{\phi_t \exp(\frac{\psi_s}{\phi_t}) - \psi_s - \phi_t} \qquad (22)$$

This is exactly (2). Hence, as in the case of an infinitely highly doped gate

$$\psi_s \approx 2\phi_t \left[\frac{V_{GB} - V_{FB} + 3\phi_t}{V_{GB} - V_{FB} + 6\phi_t} \right] \log\left(1 + \frac{V_{GB} - V_{FB}}{\gamma\sqrt{\phi_t}}\right) \tag{23}$$

C'_{gb} is calculated from

$$\frac{1}{C'_{gb}} = \frac{1}{C'_{ox}} + \frac{1}{C'_c} + \frac{1}{C'_{dep}} \tag{24}$$

where C'_c is given by (8). C'_{dep} is the capacitance of the gate depletion region per unit area. Differentiating (16), we get

$$C'_{dep} = \frac{\sqrt{2q\epsilon_s N_{POLY}}}{2\sqrt{\psi_{dep}}} = \frac{\gamma_p C'_{ox}}{2\sqrt{\psi_{dep}}} \tag{25}$$

Using (21) in the above equation gives

$$C'_{dep} = \frac{\gamma_p^2 C'_{ox}}{2(V_{GB} - \phi_{MS} - \psi_s)} \tag{26}$$

5. MEASUREMENT RESULTS AND DISCUSSION

Figure 6 compares our model with measurement results made in a modern n-well salicided CMOS processes. The gate oxide thickness for the data of Figure 6 is about 85 A. When oxide thickness is reduced to a few tens of angstroms, it has been shown that the charge-sheet model is not quite accurate. The thickness of the charge sheet and quantum mechanical effects need to be taken into account [5] [6]. If these effects are not separately modeled, the value of N_{POLY} may need to be changed to fit measurements.

6. CONCLUSION

In this paper, an explicit physics based simulation model was proposed for the MOS capacitor in accumulation. The results were compared to device simulation results and measurements. The model has been implemented in a general purpose circuit simulator (TI-SPICE), and can be used to calculate distortion in circuits.

7. ACKNOWLEDGMENTS

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APPENDIX 1

In order to find an explicit expression for ψ_s in terms of V_{GB}, we rewrite (2) as

$$\frac{V_{GB} - V_{FB}}{\phi_t} = \frac{\psi_s}{\phi_t} + \frac{\gamma}{\sqrt{\phi_t}}\sqrt{\exp(\frac{\psi_s}{\phi_t}) - \frac{\psi_s}{\phi_t} - 1} \tag{27}$$

Working with normalized variables

$$z = \frac{V_{GB} - V_{FB}}{\phi_t} \tag{28}$$

$$x = \frac{\psi_s}{\phi_t} \tag{29}$$

$$a = \frac{\gamma}{\sqrt{\phi_t}} \tag{30}$$

we have

$$z = x + a\sqrt{e^x - x - 1} \tag{31}$$

We need to find x in terms of z. Notice that the only parameter in the equation is a. If we could find an approximate explicit equation for x for practical values of a, the surface potential will "track" changes in substrate doping concentration and temperature. Then, the model formulation is based entirely on the physics of the device, and is devoid of function fitting for particular values of process parameters and temperature.

As a guide towards an approximation, we consider the asymptotic behavior of (31). For small x, the exponential can be approximated by the first three terms of its Taylor expansion, whereas for large x it becomes dominant. Thus, we obtain

$$z \approx \begin{cases} x + \frac{ax}{\sqrt{2}}, & \text{small } x \\ a\exp(x/2), & \text{large } x \end{cases} \tag{32}$$

Inverting these relations, we obtain:

$$x \approx \begin{cases} \left(\frac{a\sqrt{2}}{a+\sqrt{2}}\right)\frac{z}{a}, & \text{small } z \\ 2\log(z/a), & \text{large } z \end{cases} \tag{33}$$

The second factor in these relations can be approximated by $\log(1 + z/a)$, for both small and large z. The first factor is typically 1 for small z, and becomes 2 for large z. This behavior can be satisfied by the function $2\left(\frac{z+k_1}{z+k_2}\right)$, with k_1 and k_2 typically being 3 and 6, respectively. Thus the behavior in (33) can be approximated by:

$$x \approx 2\left(\frac{z+k_1}{z+k_2}\right)\log\left(1 + \frac{z}{a}\right) \tag{34}$$

Although this relation was developed from the asymptotic behavior of (31), we find that it approximates the latter well for the entire useful range of z and for typical values of a, when $k_1 = 3$ and $k_2 = 6$ are chosen. Thus, rewriting (34) by using (28–30), we obtain (6).

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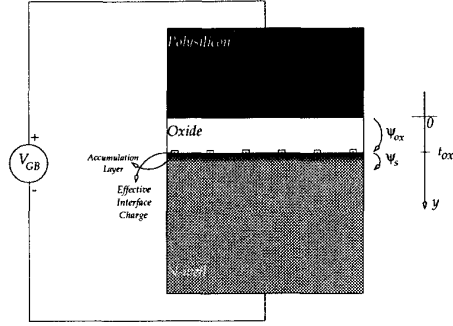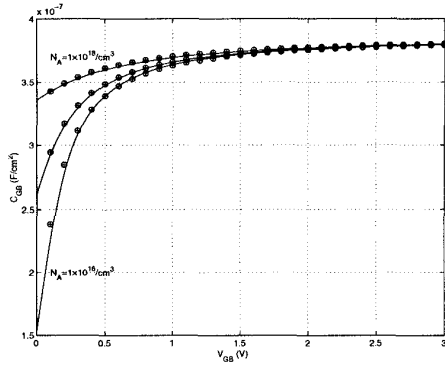
Figure 1. Cross section of an MOS capacitor.

Figure 4. 3rd harmonic relative to fundamental(−
PWL, $\oplus$ proposed model).

Figure 2. Comparison of numerical simulation and
proposed model for changes in substrate doping
concentration (− numerical, $\oplus$ proposed model)
$C'_{ox} = 3.84$ fF/μm^2, $V_{FB} = 0$, T=300 K.

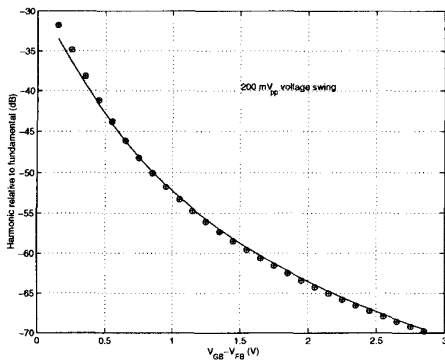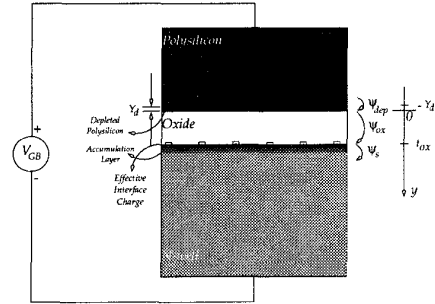Figure 5. MOS capacitor cross section indicating
the polysilicon depletion region.

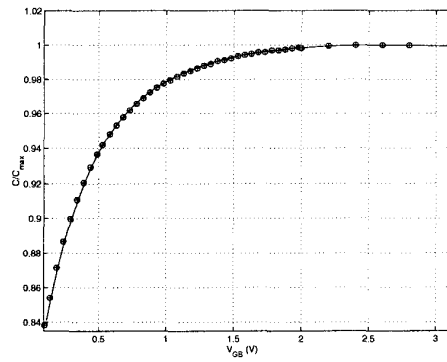Figure 3. 2nd harmonic relative to fundamental(−
PWL, $\oplus$ proposed model).

Figure 6. Comparison of complete model with
measurements, $t_{ox} = 85$ A(−model, $\oplus$ data).

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