A 46-GHz Distributed Transimpedance Amplifier using SiGe Bipolar Technology

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Abstract — **In this work we present a transimpedance amplifier (TIA) with a typical 3-dB bandwidth of 46 GHz, suitable for 40 Gb/s data communication links, realized in a commercial SiGe BiCMOS technology. The amplifier uses a traveling-wave topology and achieves a typical transimpedance of 47 dBΩ and a low input-referred current noise of 24 pA Hz$^{-0.5}$ averaged between 0 and 40 GHz. The amplifier is especially designed to be integrated with a photodiode in a hybrid photoreceiver, using bond wire interconnects. A set of photoreceivers was successfully tested over a temperature range from 0 to 70 C. The low noise of the TIA results in a large dynamic range of the receivers and error-free operation was achieved up to an overload optical input power of more than +3 dBm.**

I. Introduction

The ongoing rise of internet traffic is raising the demands for bandwidth and capacity in the backbones and nodal points of the global networks. Current approaches are exploiting wavelength division multiplexing (WDM) to combine up to 160 channels with 10 Gb/s per fiber. To reduce costs and increase capacity per channel, bit rates of 40 Gb/s are highly desirable, provided that these cutting-edge technology systems can economically compete with a 4 x 10 Gb/s solution. One step to reach this goal is the demonstration of high-speed silicon at 40 Gb/s, due to its reproducibility, maturity and reliability at minimum cost [1].

When considering the analog functions in an optical communication link, the first electrical component after the photodiode in a fiber communication system is the transimpedance amplifier (TIA). The TIA converts the photocurrent into a voltage, as shown in Fig. 1. The TIA is the first electrical amplifier in the receiver chain and thus sets the input sensitivity of the receiver after the photodiode. The high requirements on noise and bandwidth for these amplifiers were mostly met by amplifiers using

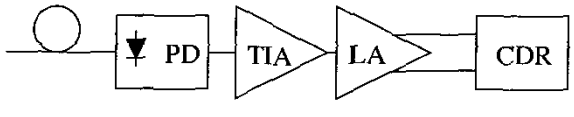

Fig. 1. Block diagram of a typical receiver chain.

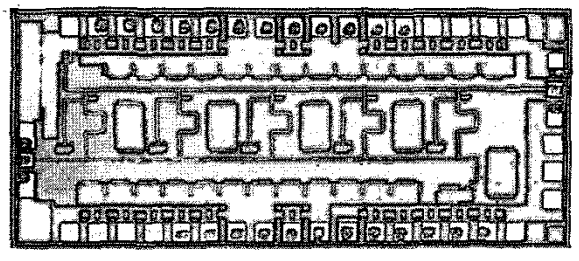

Fig. 2. Chip photograph of the distributed TIA (1.2 x 3 mm^2).

expensive III-V technologies, especially InP [2]. Nevertheless, the progression from laboratory setups to products for 40 Gb/s transmission systems raises the demand for more cost effective ICs on silicon.

In this paper, we present a fully linear transimpedance amplifier for 40 Gb/s fiber links, using a commercial 0.18um SiGe BiCMOS process [3], which is well suited for OC-768 photoreceiver applications. A traveling-wave amplifier (TWA) topology was used in order to get high bandwidth and ease the assembly with a hybrid photodiode. The TIA was especially optimized to meet the photodiode mount. The amplifier has a power dissipation of 300 mW from a single –5.2 V supply and achieves a bandwidth of 46 GHz and a transimpedance of 220 Ω. Prototype photoreceivers, that incorporate the alpha-version of this TIA and a photodiode with a responsivity of 0.6 A/W, achieved a flat frequency response with a 38 GHz bandwidth and a low integrated input-referred current noise of 5.8 μA, resulting in a large dynamic range up to +3 dBm optical input power.

II. Circuit Design

A typical photoreceiver chain is shown in Fig. 1. The photodiode and the TIA are packaged in one module to form the photoreceiver . The output signal can be amplified by a limiting amplifier (LA), which provides the required signal levels for the clock and data recovery (CDR) block. Fig. 3 shows the block diagram of the amplifier and its application in a photoreceiver. The photodiode will generate a photocurrent, which flows over a bond-wire

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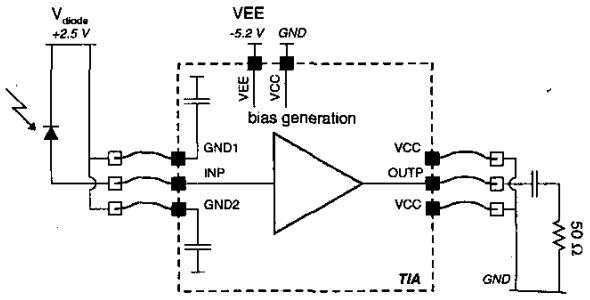

Fig. 3. Block diagram of the photoreceiver .

connection to the input of the amplifier. The output voltage signal of the amplifier is then ac coupled to a 50-Ohm termination. In our specific application, we implemented on-chip DC blocking capacitors, to allow separate biasing of the photodiode. The value of the blocking capacitance can be increased in the photoreceiver using external components, to provide the desired flat low-frequency response of this interface.

A. Circuit topology

A single-ended traveling-wave topology was chosen for the amplifier [4] to achieve the wide bandwidth necessary for 40 Gb/s data signals and also to ensure a fully linear operation of the amplifier. Five gain stages are combined with transmission lines at the input and output, as shown in the schematic diagram in Fig. 4 and in the chip photograph in Fig. 2. The die size of 1.2 x 3 mm^2 is determined by step field requirements rather than design limitations. We implemented an active load at the end of the input transmission line to set the operating point of all stages and to compensate for process and temperature variations. A significant advantage of the traveling-wave concept compared to a lumped feedback-amplifier design [5] is the insensitivity to the input load, which is highly reactive when using a photodiode and can significantly vary with the bond wire length in a hybrid photoreceiver assembly. This amplifier was especially developed to meet the needs for a hybrid photoreceiver, combining a photodiode and the amplifier using standard bond-wire connections. Fig. 5

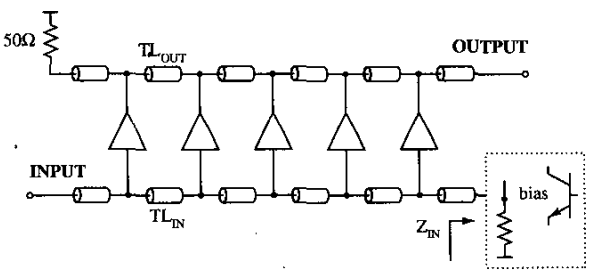

Fig. 4. Schematic diagram of the distributed TIA.

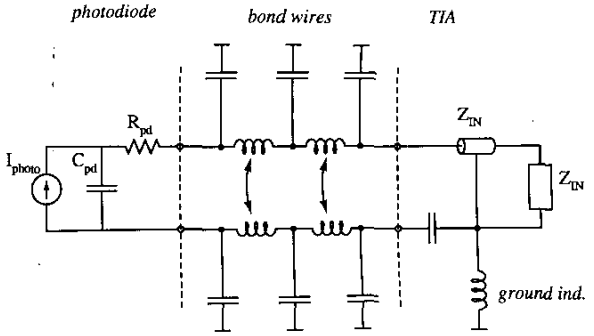

Fig. 5. Equivalent circuit model for the TIA input.

illustrates the input configuration in more detail. The photodiode, in a first approximation, can be modeled as a single capacitance with a series resistor. The bond wire is mainly an inductance. For the definition of the input characteristic of the TIA, we extended the model for the bond-wire connection using the topology shown in Fig. 5 to allow for a full 4-port configuration and to capture the influence of the DC block on the ground wires.

The input of the TIA can be modeled by a series connection of six transmission lines, which are loaded with the input capacitance of each gain stage. To obtain the desired input impedance, the simple formula for the characteristic impedance of this artificial transmission line in (1) is used, where L' and C' are the inductance and capacitance per unit length of the transmission line segments and C_{IN} is the input capacitance of each individual stage. To avoid too low an input impedance, we need to minimize C_{IN} and use high impedance transmission lines, which were realized as microstrip lines in this design. The minimum line width set by the technology design rules allows microstrip lines with up to 75 Ω characteristic impedance. The use of this minimum line width results in significant losses on the long input line of the TIA.

$$Z_0 = Z_{IN} = \sqrt{\frac{L'l}{C_{IN} + C'l}} \qquad (1)$$

B. Loss compensation

To compensate for the losses and to reduce the input capacitance C_{IN}, the gain-cell topology shown in Fig. 6 was chosen. The emitter followers EF1 and EF2 reduce the input capacitance and the transmission lines TL1 and TL2 are optimized to achieve a negative input resistance, similar to the method presented in [6]. This is illustrated by the Smith chart in Fig. 7, which shows an input reflection coefficient $S_{11} > 1$. Furthermore, the use of transmission lines to generate band-limited feedback within the cascode configuration of transistors T1 and T2 results in a broadband and well-controlled peaking characteristic in the

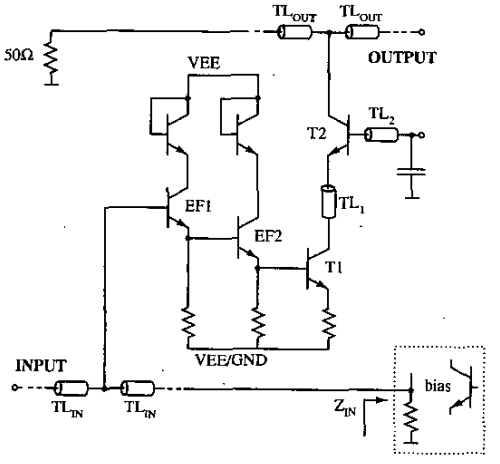

Fig. 6. Schematic of the gain cell.

frequency response of the amplifier. This configuration is less sensitive to potential instabilities especially at the cut-off frequency of the amplifier, as compared to the commonly used inductive peaking, which introduces an inductive element or transmission line section at the output of the gain cell. The output reflection coefficient S_{22} is also highly reflective.

Since this method needs reliable modeling of the transmission lines to prevent instabilities, we developed accurate models for the passive structures and implemented these in both Agilent ADS and Cadence design environments. Various geometries of microstrip lines were simulated in electromagnetic field simulators (Ansoft HFSS and SONNET), and scalable models using lumped and distributed circuit elements were generated based on the simulated s-parameters.

III. Measured Results

A. Amplifier characterization

The amplifier was first electrically characterized by measuring s-parameters on the die-level. Ground-Signal-

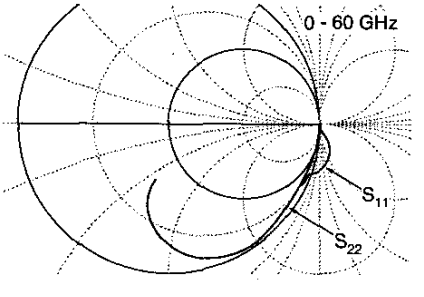

Fig. 7. Input and output reflection coefficients of the gain cell.

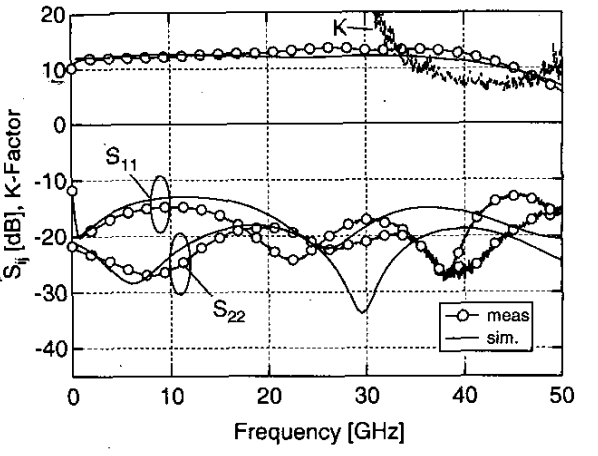

Fig. 8. On-wafer measured and simulated s-parameters and measured stability factor K of the TIA.

Ground probes were used on the probe station, allowing for reliable calibrations to the probe tips up to 50 GHz. The s-parameters were taken by a 50 GHz VNA system (HP8510C). We carefully controlled the input power to be sure not to drive the amplifier into saturation. The measured and simulated s-parameters are shown in Fig. 8. Good agreement could be achieved. The amplifier is unconditional stable as indicated by the K-factor and the reflection coefficients plotted in Fig. 8. The input-referred current noise spectrum and the group delay of S_{21} was also measured and is illustrated in Fig. 9. The spectral noise is less than 32 pA $Hz^{-0.5}$ up to 40 GHz, with an average

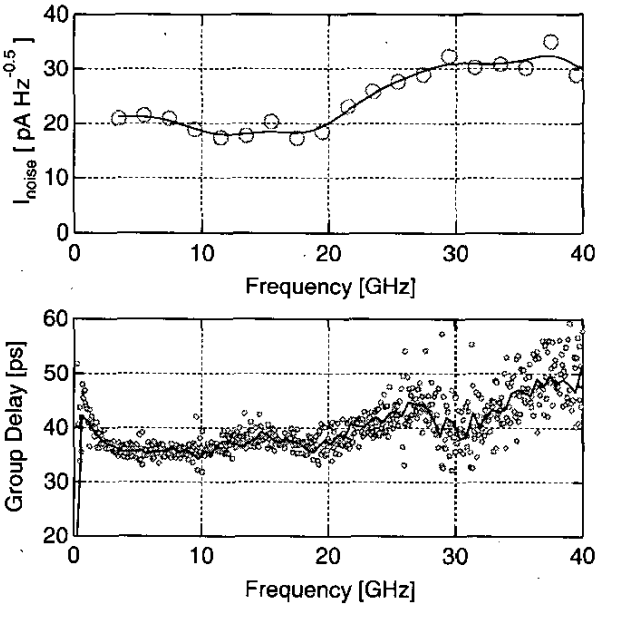

Fig. 9. On-wafer measured input-referred current noise and group delay of the TIA.

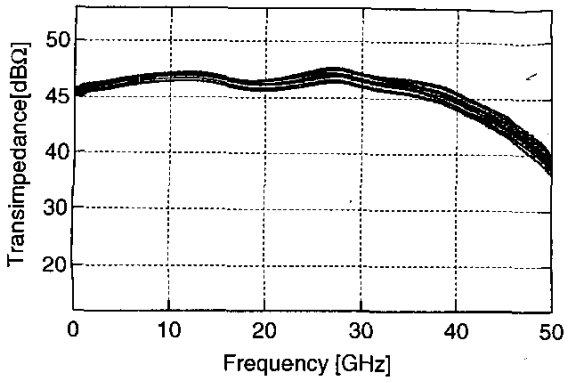

Fig. 10 Measured transimpedance of 15 representative TIAs.

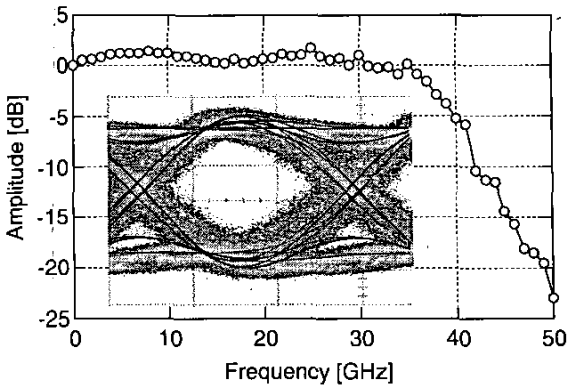

Fig. 11 Photoreceiver transfer characteristic and eye diagram.

density of 24 pA $Hz^{-0.5}$, and a group-delay ripple of about 10 ps.

More than 50 dices were measured and sorted for further integration into photoreceivers. All devices were fully functional and well within the specifications required for OC-768 photoreceivers. The average bandwidth of the measured TIAs was 46 GHz for an average transimpedance 47 dBΩ. Fig. 10 shows transimpedance measurements of 15 representative amplifiers calculated from the s-parameters using matrix transformations.

B. Photoreceiver characterization

A set of prototype photoreceivers using a photodiode and this TIA, with pigtailed optical input and V-connector output, were also tested. A typical frequency response and eye diagram is given in Fig. 11. This photoreceiver uses the first generation of the presented TIA with a slightly reduced bandwidth of 40 GHz and higher peaking at the cutoff frequency. The design of the new amplifier reduces this overshoot and jitter.

Nevertheless, the photoreceiver passed an initial BER test in an unoptimized test bed and we achieved error free operation. The overload performance was also measured and a maximum optical input power of more than +3 dBm can be accepted by the receiver. From the measurement of the output noise voltage and the transimpedance, we calculated an integrated input-referred current noise of about 5.9 μA, which corresponds to the on-wafer measured average input-referred current noise of 24 pA $Hz^{-0.5}$ of the TIA. The performance of the photoreceiver was verified from 0 to 70 C case temperature, proving the functionality of the temperature-compensated bias circuitry.

V. Conclusion

We have presented a distributed transimpedance amplifier fabricated in a production SiGe BiCMOS process. The bandwidth of 46 GHz, 47 dBΩ transimpedance, an average input-referred current noise of 24 pA $Hz^{-0.5}$, and a flat frequency response enabled the production of a high performance photoreceiver. Reproducibility was demonstrated, making this chip a low-cost high performance product for OC-768 applications.

Acknowledgement

The authors would like to thank Carlos Bowen, Jason Cancio, Fred Sugihwo, Sumit Verma and David Pritzkau for layout and testing.

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