

A 60-350 MHz Programmable Analog Filter in a Digital CMOS Process

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Abstract

We present a programmable fourth-order Butterworth continuous-time filter with a bandwidth programmable from 60-350 MHz, implemented in a 0.25 μm digital CMOS process. It is intended for communication and mass storage applications. The filter has a dynamic range of 54 dB, dissipates 70 mW from a 3.3 volt supply and occupies an area of 0.15 mm². Suitably biased accumulation MOS capacitors are used as integrating elements.

1. Introduction

High-speed communication and storage systems need continuous-time filters with bandwidths tunable over a wide range, while keeping the shape of the frequency response identical irrespective of the set bandwidth [1], and maintaining an adequate dynamic range. For high levels of integration and to reduce cost, it is desirable to implement these filters in deep-submicron digital CMOS technologies. Filter pole frequencies in the hundreds of megahertz range demand that the parasitic poles in the integrators be in the gigahertz range. Conventional techniques would consume large amounts of power in such operation. In this paper, we present a high-frequency continuous-time filter technique which is specially suited for deep-submicron CMOS implementation. We take advantage of the fact that, at the signal levels required (about 200 mV pp diff) no linearization is needed for the transconductors, and (inherently nonlinear) MOS accumulation capacitors can be used [2] as the integrating elements in place of the large metal-metal capacitors typically employed on digital CMOS processes. To allow frequency scalability without deterioration of noise and of the frequency response shape, we employ "constant-capacitance scaling", as explained below.

2. Constant-C Scaling

Consider any network consisting of transconductances, conductances and capacitors, and let the voltage transfer function between any two nodes $n1$ and $n2$ be denoted

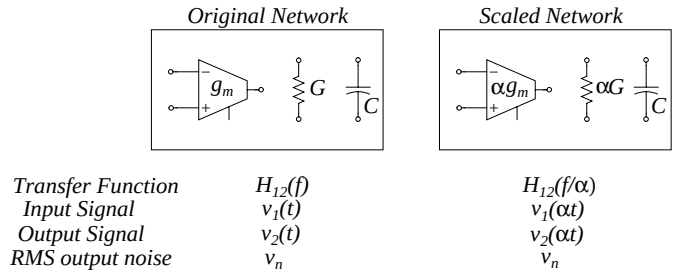


Figure 1. Properties of scaled networks

as $H_{12}(f)$. If **every** conductance and transconductance in the network is multiplied by an arbitrary number α while keeping **every** capacitance the same, then it is easy to show that the voltage transfer function between $n1$ and $n2$ is changed to $H_{12}(f/\alpha)$. We call the above modification constant-C scaling. It corresponds to a stretching of the frequency axis. It can be shown [3] that under constant-C scaling, the integrated output noise of the network at any node is independent of α . The important properties of constant-C scaled networks are shown in Figure 1; the second and third lines of the table in that figure mean that if an input $v_1(t)$ applied to the original network produces an output $v_2(t)$, then applying $v_1(\alpha t)$ to the scaled network produces $v_2(\alpha t)$. It can be shown [3] that this holds even if the capacitors are nonlinear. From this it can be shown that the worst case harmonic distortion of a constant-C scaled filter under sinusoidal excitation is also independent of α . This has profound implications in filter design: if the original filter is designed optimally in terms of thermal noise and distortion, then any constant-C scaled version of it will also be optimal, irrespective of frequency setting. This property is key to making possible the performance of the chip described in this paper. Consider now the simplified schematic and symbol of a unit transconductance element shown in Figure 2. (In the actual circuit cascoded PMOS devices were used.) M1, M2, M3 and

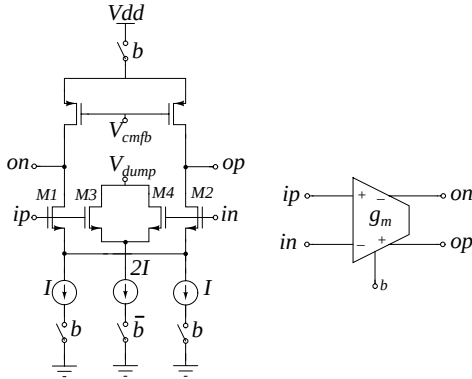


Figure 2. A unit transconductance element

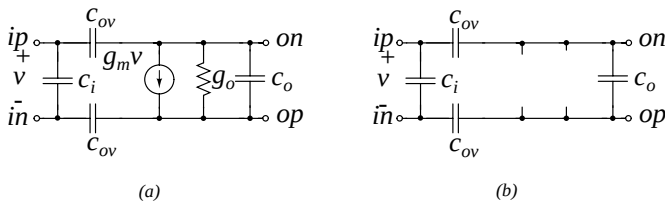


Figure 3. The small-signal equivalent circuit of the transconductor of Figure 2 under differential excitation, for the cases (a) $b = 1$ and (b) $b = 0$ (where b denotes the state of the corresponding switches in Figure 2)

M4 are identical devices. M3, M4 are dummy devices used to maintain a constant input capacitance irrespective of the state of the switches. V_{cmfb} is a common-mode feedback signal, the generation of which is discussed in a later section. b and $\bar{b}$ are complementary switches. The small-signal equivalent circuits for differential excitation for the cases $b = 1$ and $b = 0$ are considered in Figure 3 (a) and (b) respectively. In (a), M1-M2 operate in strong inversion while M3-M4 are off. In (b), M3-M4 operate in strong inversion while M1-M2 are off. In **both** cases, **all** nodal capacitances in the network remain identical. Notice that when the transconductor M1-M2 is turned off, **every** transconductance and conductance in the network is scaled by α (where $\alpha = 0$ in this case), while **every** capacitance remains the same. Also, the transconductor M1-M2 does not contribute noise when it is turned off.

Now consider the parallel connection of two identical unit transconductors as shown in Figure 4. The table in the figure lists the various parameters of the composite transconductor (denoted by G_m , C_o etc.) as a function of those of the individual transconductors. Again, note that **every** node capacitance remains the same while **every** transconductance/conductance scales appropriately. The results can be extended to many unit transconductors connected in parallel.

3. Filter Architecture

For programmability, the composite transconductors used in this work are binary-weighted arrays, each consisting of 19 unit transconductors as shown in Figure 5. When the digital word corresponding to $b_0b_1b_2b_3$ is set

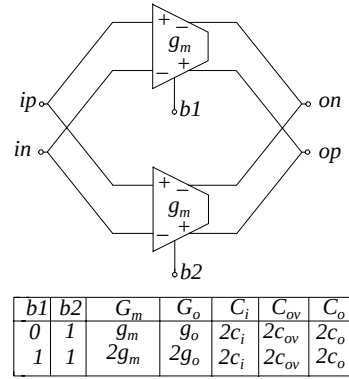


Figure 4. Parallel connection of two unit transconductors

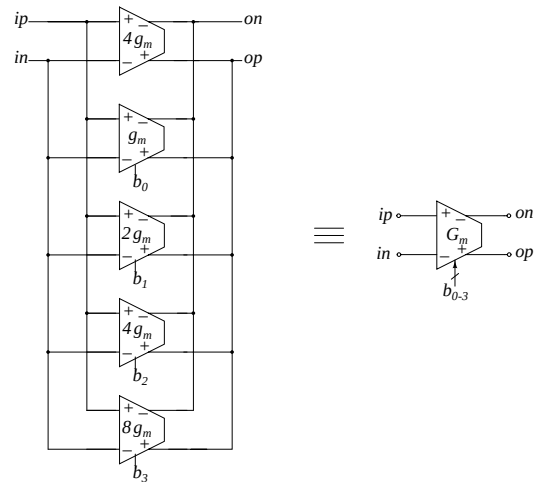


Figure 5. 4-bit programmable transconductor

to 0000, only four unit elements are switched on. When the word is 1111, all 19 unit elements are on. The coarse programming range is therefore $19/4 = 4.75$. A simple calculation will show that if $1/f$ noise is neglected, the input referred noise of the transconductor is independent of the number of unit cells that are on. Another useful feature is that the DC gain of the composite transconductor remains constant irrespective of the digital word.

The filter consists of two second order filter sections, of the type shown in Figure 6. All transconductors are made equal-valued for matching reasons. Common-mode feedback circuits (see below) are used to set the common mode voltage of every set of balanced nodes to 1.2 volts. The integrating capacitors are grounded MOS accumulation devices made of n -poly- n -well structures biased at 1.2 V. These capacitors also serve as compensating capacitors for the common-mode feedback loops. Since the integrating capacitors and the parasitic input capacitance of the transconductors are both formed from gate oxide, a good degree of matching of capacitor ratios can be expected.

4. Common-Mode Feedback

Figure 7 shows the common-mode feedback circuit. The differential pair, consisting of M1-M2 (operated at

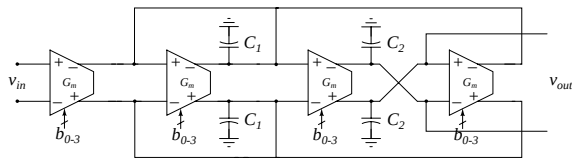


Figure 6. A second order section

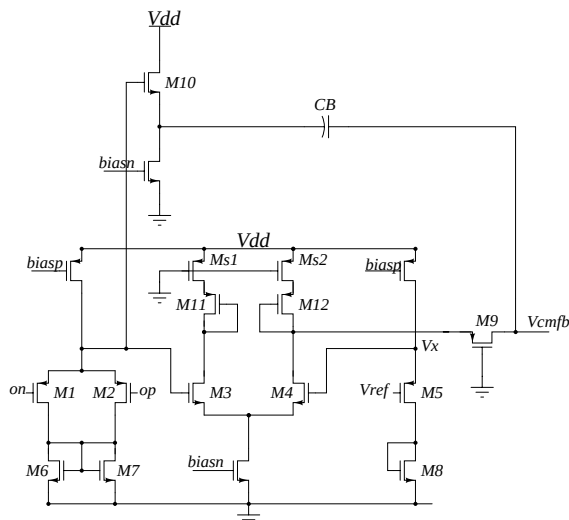


Figure 7. Common-mode feedback circuit

a large gate overdrive voltage), forms the common-mode detector. An advantage of this kind of detector is its capacitive input impedance. The detected common-mode voltage is compared with a common-mode reference (V_{ref}) which goes through a PMOS source follower (to mimic the common-mode detector). M3, M4, M11 and M12 form the servo amplifier. M10 is a low output impedance source follower. M9 is a p-channel device operating in the triode region. Along with CB, it acts like a cross-over network between the servo amplifier and the source follower. This arrangement allows a high DC loop gain at low frequencies while providing a feedforward path at high frequencies. CB is a large capacitor realised using an accumulation MOS structure. Ms1 and Ms2 are replicas of the corresponding devices used as the top switch in the transconductor of Figure 2. To keep the filter bandwidth invariant with temperature, the transconductance of every differential pair in the filter is servoed to a precise external resistor.

5. Experimental Results

The filter was fabricated in a $0.25\text{ }\mu\text{m}$ n -well digital CMOS technology. Fig. 12 shows the photograph of the filter test chip. The active area is 0.15 mm^2 . A power supply voltage of 3.3 V was used. The test setup used was similar to that used in [4]. Figure 8 shows the pass band detail of the filter for various settings of the frequency control word. As can be expected, the response scales cleanly, thanks to the constant-C technique described above. Figure 9 shows the stopband performance of the filter for different frequency settings (in interpreting these plots, note

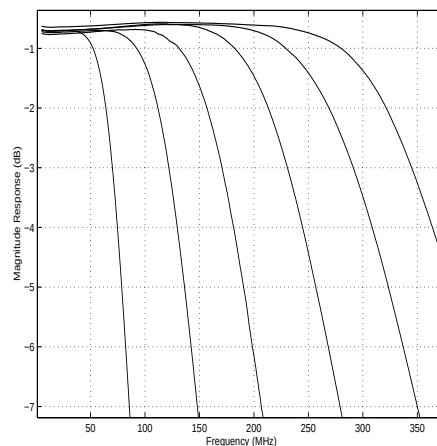


Figure 8. Passband detail for some frequency settings

that the frequency axis is linear). Figure 10 shows the response of twenty filter chips overlaid on the same plot, with the external resistor set to the same value. There are two reasons for measuring the response at the low-end bandwidth. First, this corresponds to the worst case because only the minimum number (4) of unit transconductance cells are turned on. Hence mismatches in response will be most obvious. Second, at low bandwidths, the mismatch in the test buffer paths can be expected to be very small and hopefully negligible. The mean bandwidth and standard deviation of the twenty chips measured was 59.97 MHz and 0.5 MHz respectively. These results attest to the fact that the response is very repeatable over a number of chips. The noise spectra of the filter and buffer paths from 10 MHz to 150 MHz is shown in Figures 11. The filter output noise spectrum is shown for two different bandwidth settings - the top trace is for the case when the digital bandwidth setting code is 0000 (corresponding to a filter bandwidth of 75 MHz) while the bottom trace is for a code 0010 (bandwidth = 112 MHz). As predicted by frequency scaling theory, the output noise power of the filter at very low frequencies reduces by $10 \log(112/75) \approx 1.75$ dB as the bandwidth is increased by a factor of $112/75$. A summary of measured results is given in Table 1.

6. Conclusions

An architecture for the realisation of very high frequency CMOS continuous time filters has been presented. Simple differential pairs and MOS accumulation capacitors have been used to reduce area and noise, and to allow proper frequency scalability. These techniques were demonstrated with a prototype fourth-order Butterworth lowpass filter tunable from 60-350 MHz while consuming 70 mW from a 3.3 volt supply. A 0.25 μm *n*-well digital CMOS technology was used.

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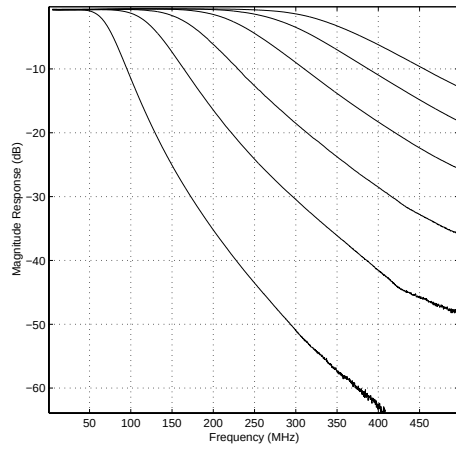


Figure 9. Stopband response for some frequency settings

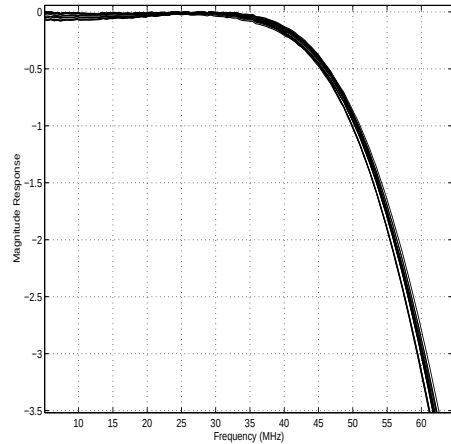


Figure 10. Response of 20 filters measured under identical conditions (lowest bandwidth setting). Mean bandwidth = 59.97 MHz, Standard Deviation 0.5 MHz

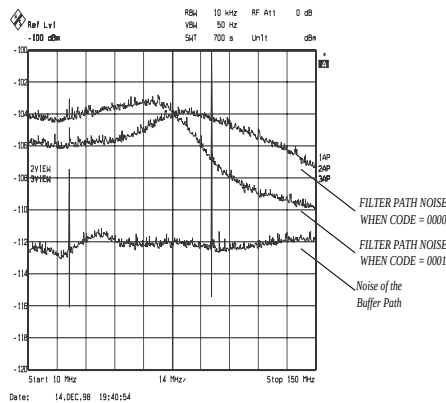


Figure 11. Filter noise spectrum

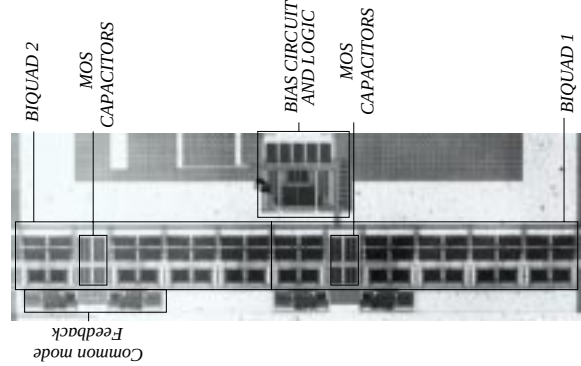


Figure 12. Chip Microphotograph

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Table 1. Summary of measured characteristics (25°C)

Technology	0.25 μm n-well CMOS
Filter Type	4 th Order Butterworth
Supply voltage	3.3 V
Cutoff Frequency Programmability	60–350 MHz
Chip area	0.15 mm ²
Power (All bandwidths)	70 mW
DC gain	−0.8 dB
Integrated Output noise	257 μV , rms
f_{-3dB} variation for V_{dd} 3 – 3.6V	$\pm 2\%$
Test tone at $f_{-3dB}/3$:	
$V_{i pp, max}$ (THD ≤ 40 dB)	380 mV
Dyn. range (THD ≤ 40 dB)	54 dB

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